Barry's SS-150 Motherboard Design 5th Generation

by

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Introduction

I would like to take the time in Thanking each and everyone of you for reading this Science and technology based work. I have made improvements on the SS-125 Motherboard Design please view the following below:

a). Data Strings 8 strings per chip 8192 bits per string total 40 strings total 65536 per chip total bits 40 * 65536=327680 buffer holds 40960 total = 368640 bits
b). Quad Core CPU CPU 1-3 (12 layers) and CPU 4 (9 layers) asymmetrical total bits 368640 bits
c). CMOS with color spectrum to match CPU Processor's 1-3 Red 4 yellow
d). New Cryptographic Energy Model Multiple Path Processing and Red Encapsulation
e). 8 bridge wiring scheme 8192 bits memory chip
f). **8192 Bit CPU Pin Grid array**
g). CPU 1-4 have fiber Optic Encased Wiring (Input)
h). Voltage Regulator now has 8* 1024 bits wires with 8192 terminator block switch
I). Buffer Chip to interface between BIOS and CPU avoid I/O overflow
J) Memory Chips have wires that are encased using Fiber Optics
K) CPUs also have wires that are encased using Fiber Optics using Input only

1). The Visual **Model Super Sonic 150 Motherboard 1-A General View** overall view of the product and demonstrates a Industrial Design because of it's unique characteristics. The detailed features that are within the Design accompanies in views 1-a through 10-A with detailed specs. The features of this design comes with Asymmetrical four intertwined CPU's 1-3 and have 12 layers each also CPU 4 has 9 layers total bits **368640 and 45 layers** . Color spectrum's Red and Yellow are used to interface with various components example is CMOS wired to the CPU's. This CPU Asymmetrical Design now has the ability to use 8192 bits instead of the standard 4096 bits to the clipboard. The memory chip has 8 wires for the Data bridges to push through 8192 bits establishing equilibrium between the CPU and Memory in terms of bits. Terminator blocks with switches are now being implemented that interface between the CMOS and CPU this allows for better I/O control of system processing along with a buffer chip to prevent overloads.

2). **Patent Ideal 2 Method and Single 368640 Data Block processing. T**his is discussed as a method and process of Internal Packet exchanges within the Motherboard Design itself and is upgraded as well.

3). **Patent Idea New Cryptographic Energy Model Design-Crypt 1300-1700 model.** This is shown as an Industrial Design along with the method and process. This comes with dynamic bit data strings, linear and dual curvature elliptic circles with password encryption and padding Mathematical equation with process, method and dynamic heat via color spectrum schemes.

4). I have updated the Video card and slot that now supports the Crypt 1300-1700 model with no more PKCS 12 and now has dual elliptic curvatures that run clockwise and counter clockwise motion with dual blade fans

5). I have updated some components on the Motherboard to use a ring 24 Star Network Topology Design including the video Card, adapters, and fans use a single or double bladed 24 star creating a 48 point node point on the fans itself

6). Built in Hardware Certificate now includes the Crypt 1300-1700 Model 40960 bits also I have added a color spectrum scheme to run the dual bridge choosing the correct path to send data. The Crypt 1300-1700 now has red and orange spectrum's with the red having fiber optic wiring and encapsulation of data.

7). I have updated most major components on this motherboard with Fiber Optics CPU's, Memory Chips, etc.. this allows for me to represent future designs in Nanobits. This design is represented in bits, bytes, characters.

This is a 5th generation motherboard Design. Once again thank you for reading this work !

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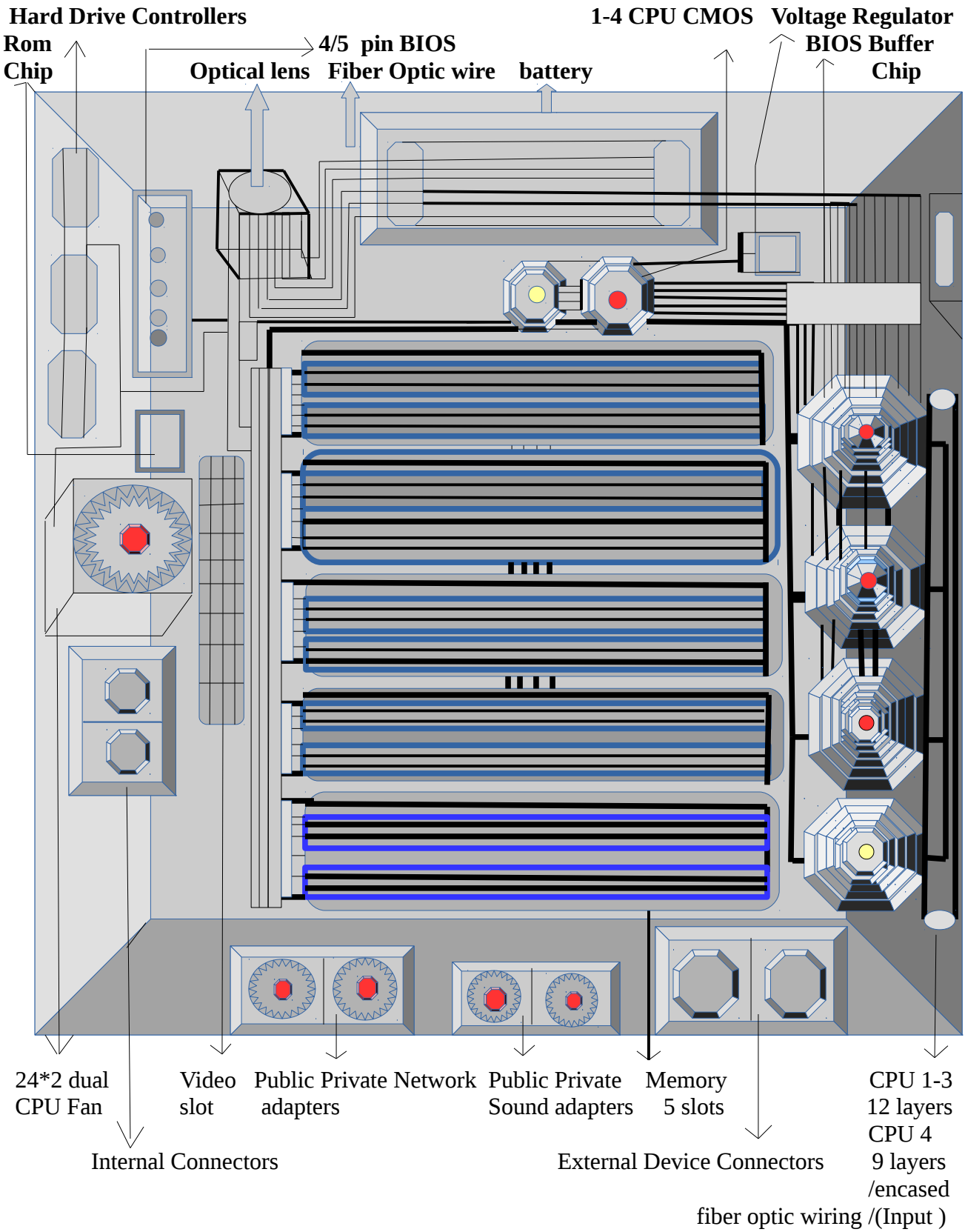
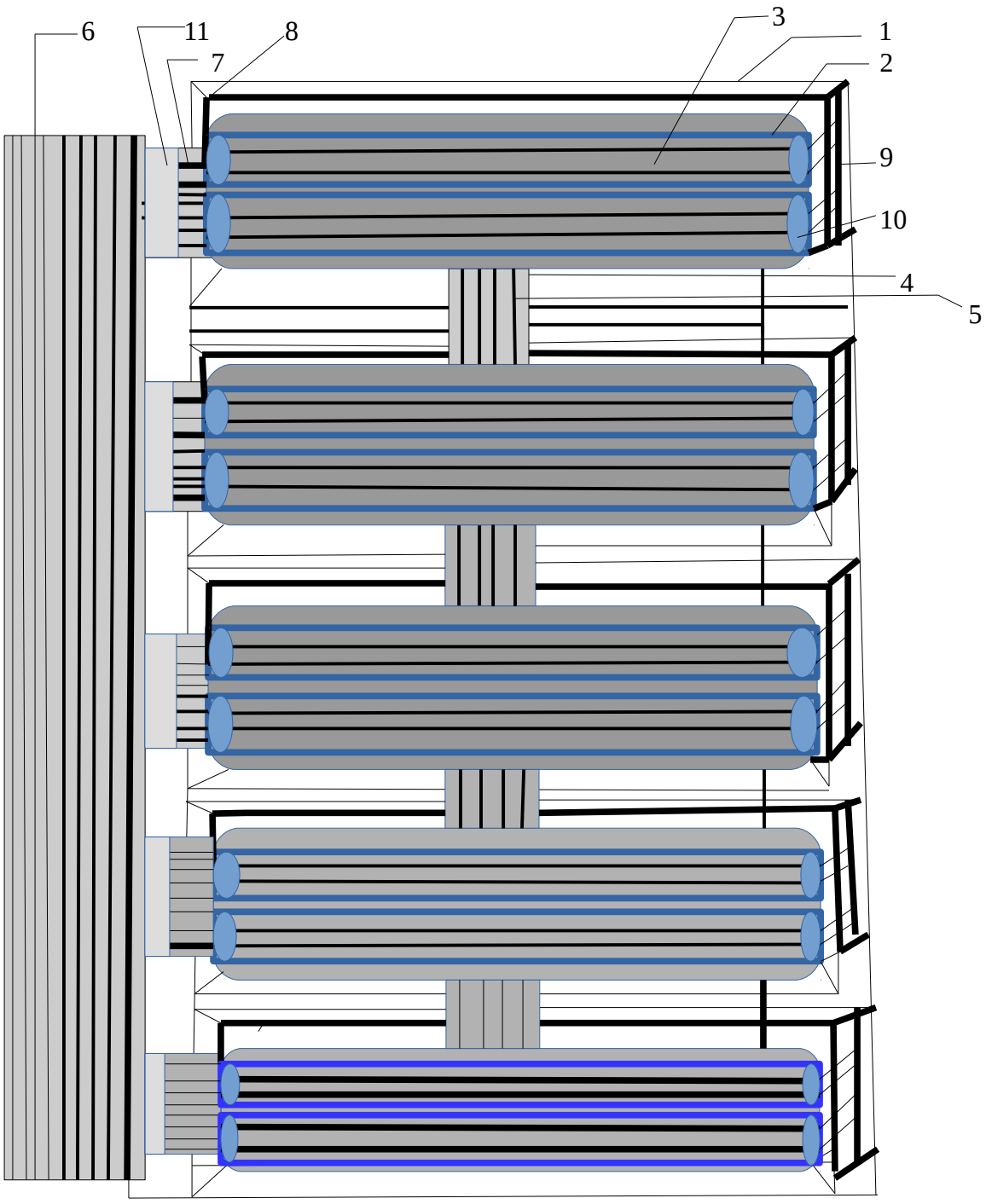
Model Super Sonic 150 Motherboard- Design 1-A General View



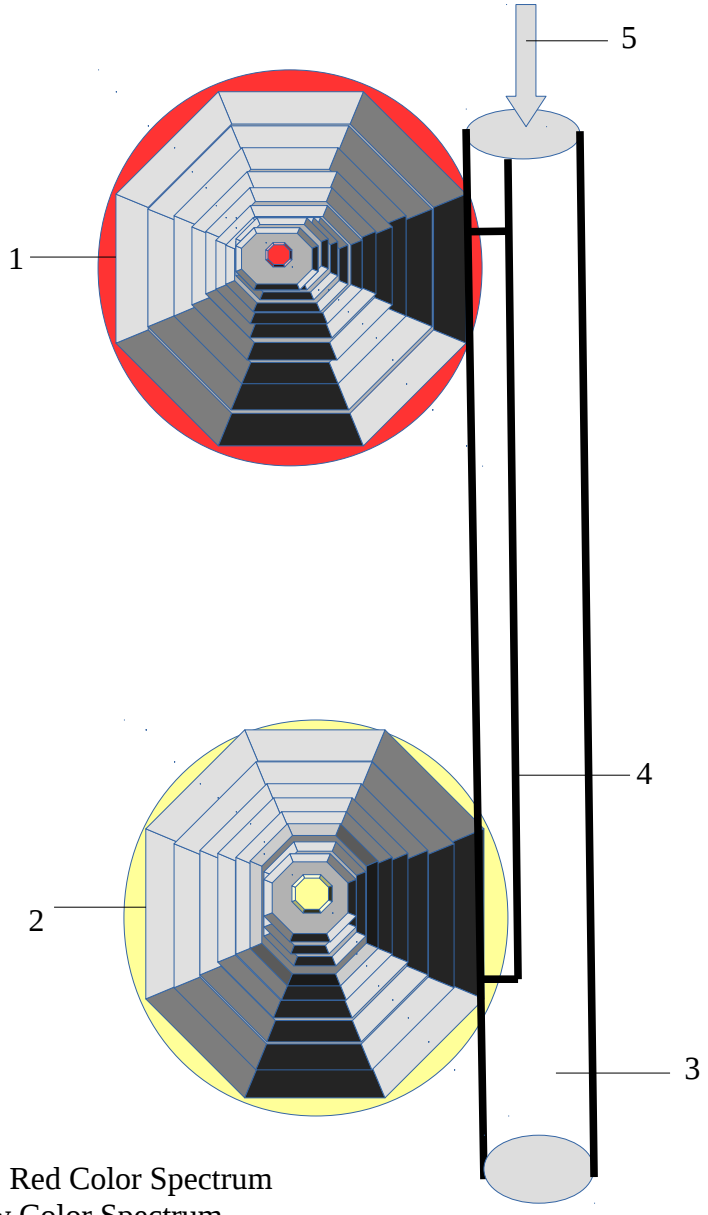
Model Super Sonic 150 Dual memory Core General View 2-A



1). Fitting to hold Memory Chips
2). Banks 4 banks per Dual Core memory chip 20 banks total
3). Data Strings 8 strings per chip 8192 bits per string total 40 strings total strings per chip 8 * 8192 = 65536 total strings 40 * 8192 = 327680 buffers holds 40960 see number 11
4). Area Memory Bridge (Bytes to Frames switches)
5). 8 data strings per bridge 8192 bits per wire total 65536 bits

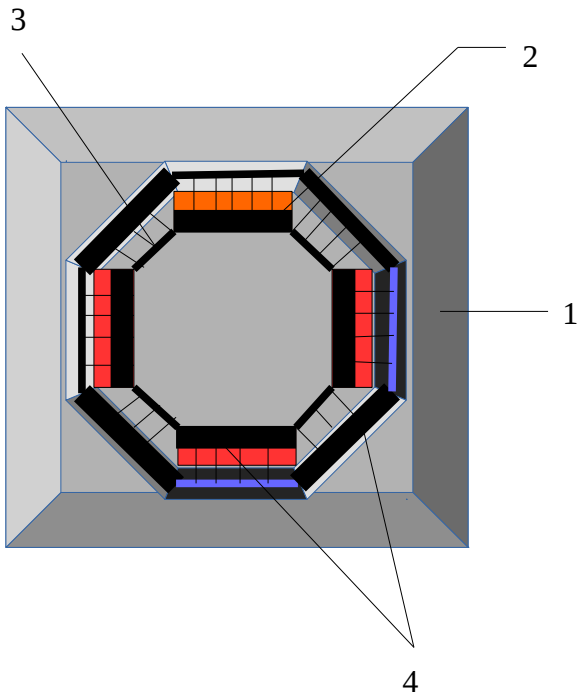
6). Fiber Optic tube address encasement 5 wires
7). Address Bridge 8 wires 8192 bits per wire to process Fiber Optic
8). Dual Core Memory Chips
9). Terminator block 4 wires per chip
10). Fiber Optic tube
11). Memory Buffer (Temporary storage) holds 40960 5 buffer chips 40960 /5 =8192 per chip

Model Super Sonic 150 CPU and Topology Design General Views



1). CPU 1 - 3 Layers 1-12 Red Color Spectrum
2). CPU 9 Layers 9 yellow Color Spectrum
3). Fiber Optic Case (Input)
4). Fiber Optic wiring
5). Direction flow of Data Input

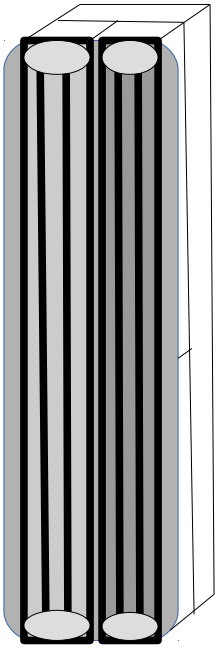
Model Super Sonic 150 CPU Octagon 8192 Pin Block Array



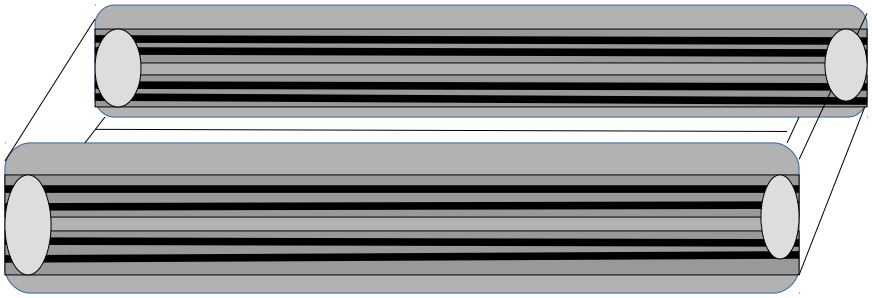
1) CPU Fitting
2). Pins into the CPU Fitting 4 Sets =4096 bits
3). Pins out to the CPU Fitting 4 Sets = 4096 bits
4). CPU total Pins into and out into CPU 8192 bits

Model Super Sonic 150 Motherboard memory Front and Side View 2-A

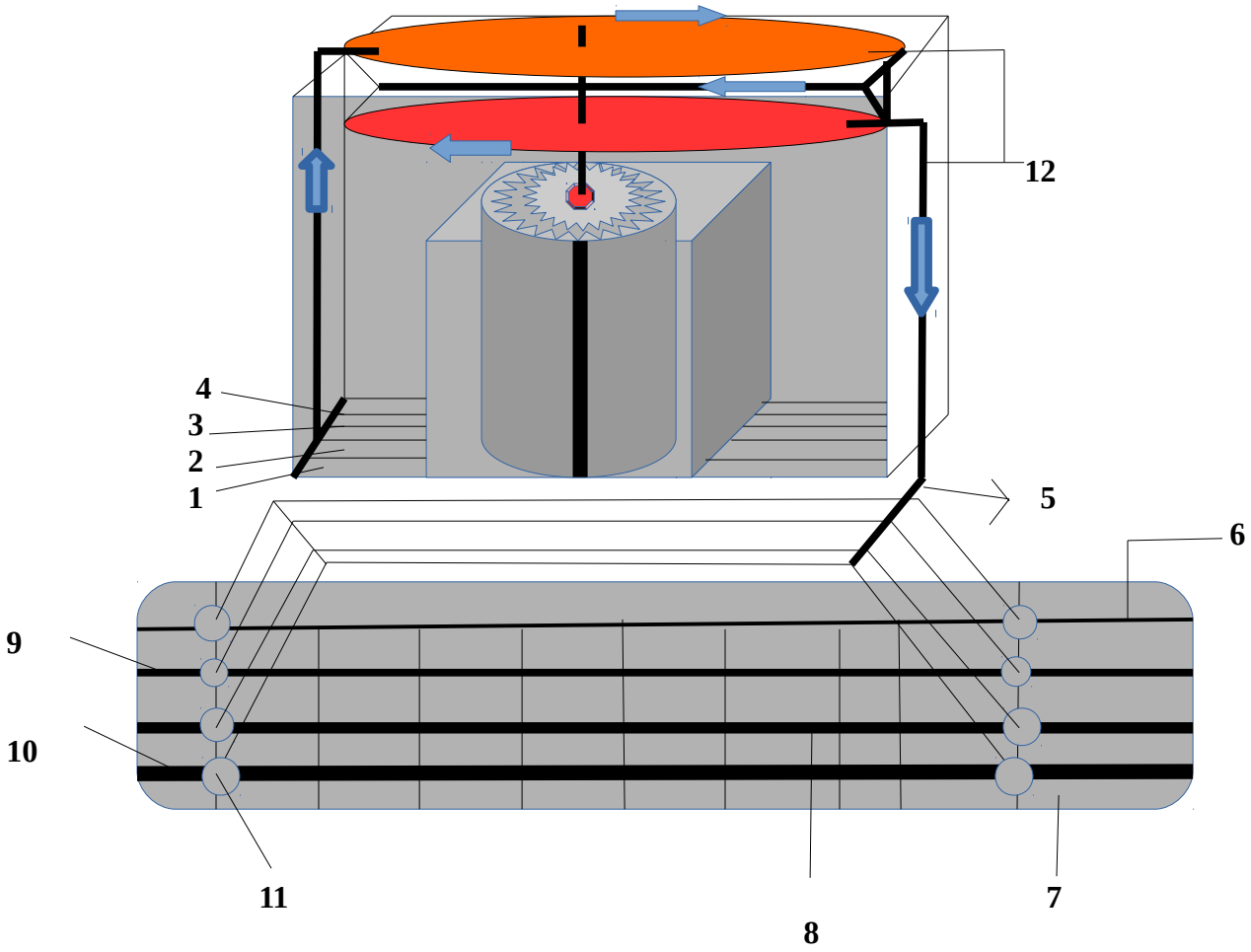
Dual Core



Dual Core Memory Front View

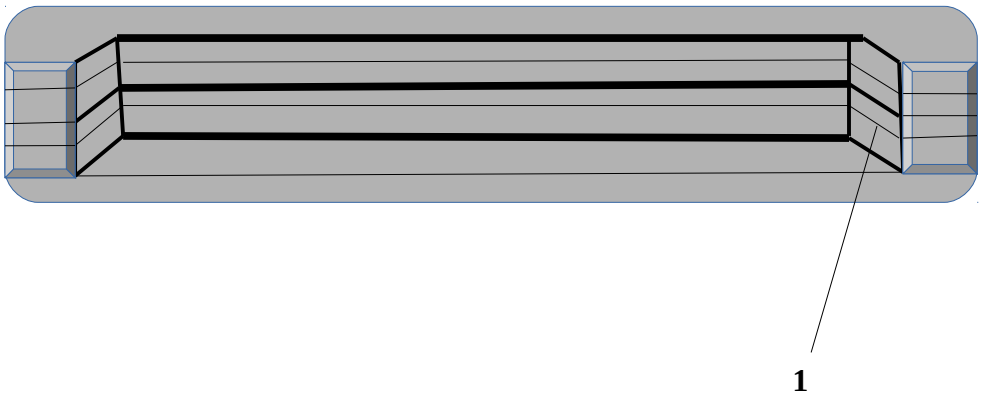


Model Super Sonic 150 5th generation Industrial Video /Fan Idea 4- A General View



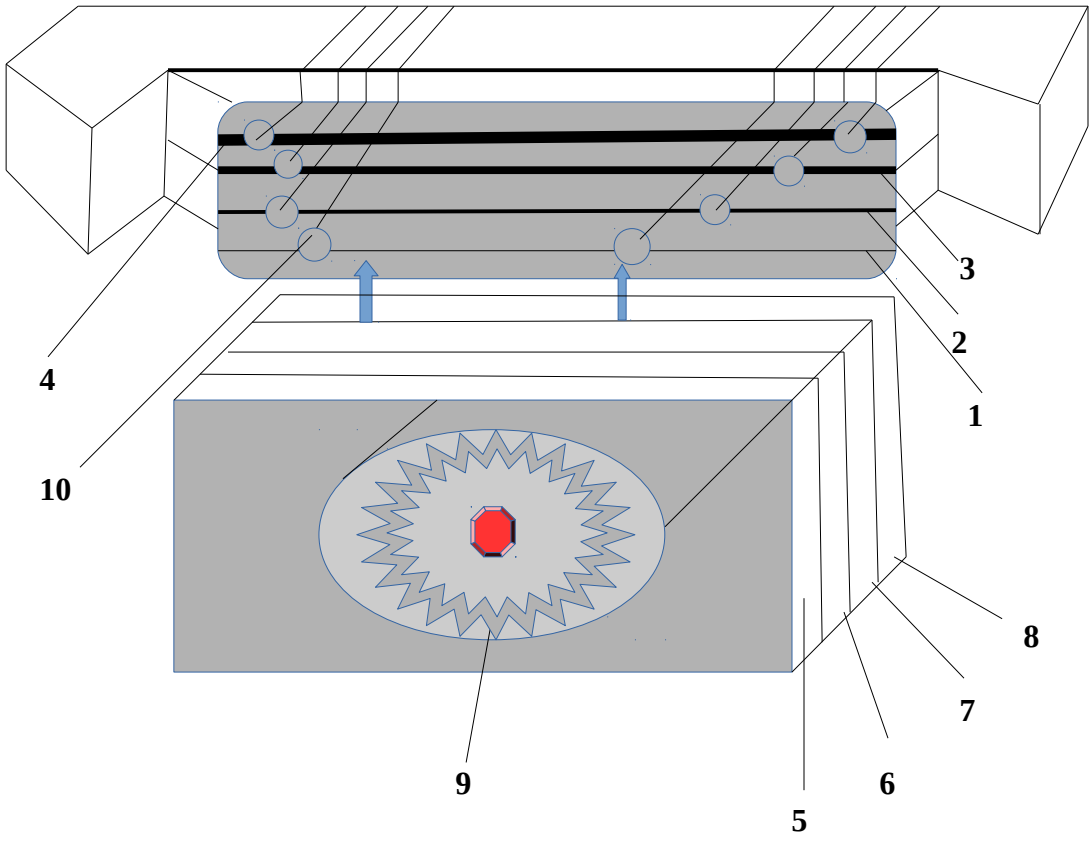
1). Public Video Area Crypt 1300-1700 model
2). Private Video Area Crypt 1300-1700 Model
3). Shared Video Area Crypt 1300-1700 Model
4). Reserved Video Area Crypt 1300-1700 Model
5). Video Data Bride 4 slots
6). Public Data String
7). Titanium video fitting
8). Shared Data String
9). Private Data String
10). Reserved Data String
11). Node Points (End to End point connection)
12). Crypt 1300-1700 Model energy regeneration

Model Super Sonic 150 5th Generation Industrial Patent video slot 5-A General View



1) **Side view of the slot where the Video Card is placed.**

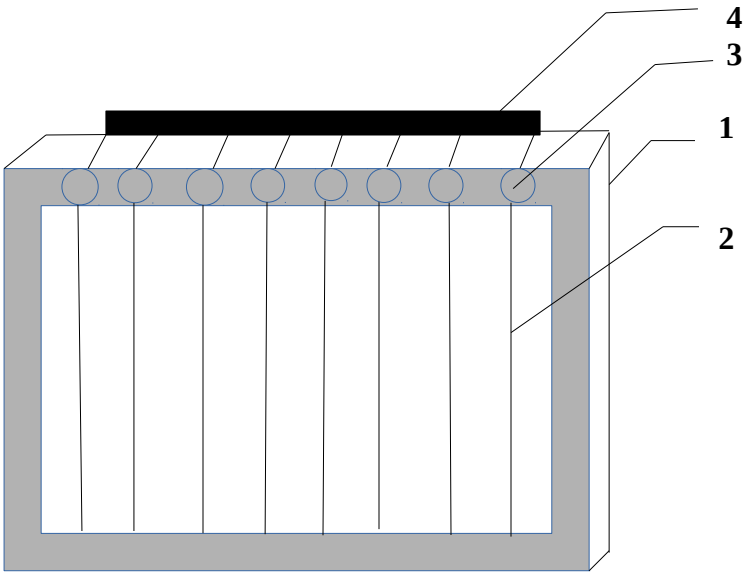
Model Super Sonic 150 5th Generation Industrial Video slot specs Idea 6-A General View



1	**Public Data String Crypt 1300-1700 Model**
2	**Private Data String Crypt 1300-1700 Model**
3	**Shared Data String Crypt 1300-1700 Model**
4	**Reserved Data String Crypt 1300-1700 Model**
5	**Public Video Slot**
6	**Private Video Slot**
7	**Shared Video Slot**
8	**Reserved Video Slot**
9	**Video Fan Double bladed 24 points * 2 = 48 Points**
10	**Node Points**

Model Super Sonic 150 5th Generation Industrial Idea 7-A General View

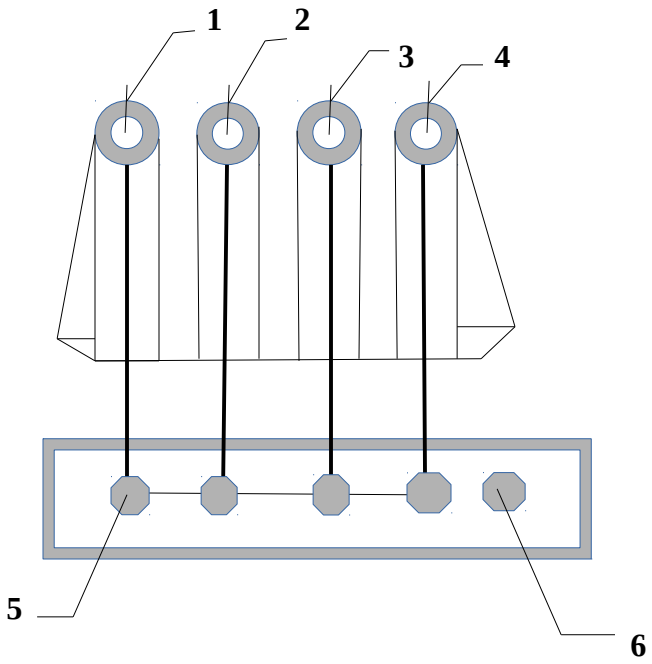
Voltage Regulator 8 wire Check



1). Overall view of chip
2). 8 wires inside chip to check flow of voltage 1024 bits per wire total 8192 bits
3). Node Point check testing wires for on and off conditions
4). Terminator Block

Model Super Sonic 150 Industrial BIOS Idea 8-A General View

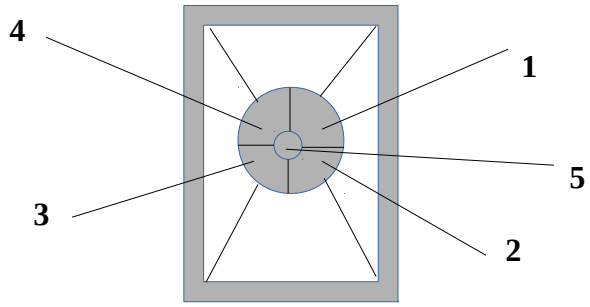
4/5 Pins BIOS



1). Public BIOS Pin
2). Private BIOS Pin
3). Shared BIOS Pin
4). Reserved BIOS Pin
5). BIOS Bins that connect to node Points
6). BIOS Pin Clearing areas of spaces

Model Super Sonic 150 5th generation Industrial ROM Chip Idea 9-A General View

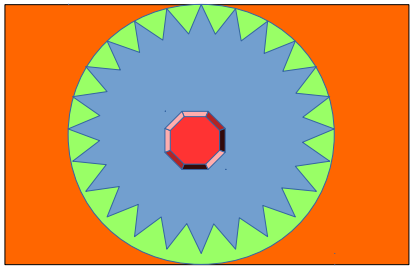
Encrypted -Crypt 1300-1700 Model Built in Certificate ROM Chip



1). Public Area of Space
2). Private Area of Space
3). Shared Area of Space
4). Reserved Area of Space
5). Certificate on burned on platter read only

Model Super Sonic 150 5th Generation Industrial Rom Chip specs Idea 10-A General View

Barrys Scientific Based Products Encrypted -Crypt 1300-1700 Model

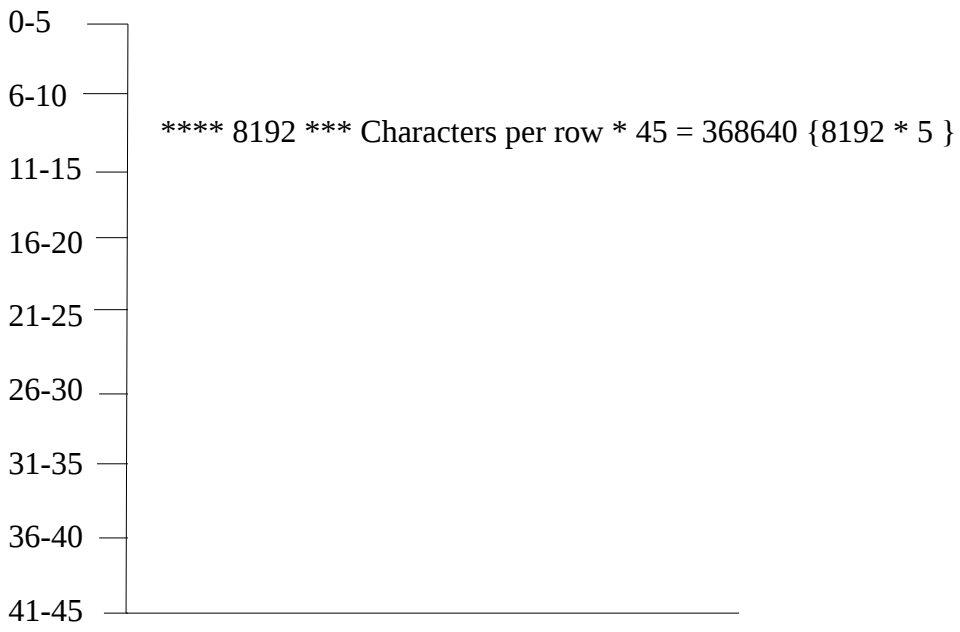


This Certificate is used to check for authenticated Hardware updates it is built into the motherboard via ROM Chip to access the Certificate which is capable of 40960. This is derived from the number of cycles produced by both linear and elliptic bits produced within the Internal encryption mechanism. I did not include the bridges in this because of using different paths with different energy levels being produced see chapter 3.

Chapter 2

Single 368640 Data Block processing

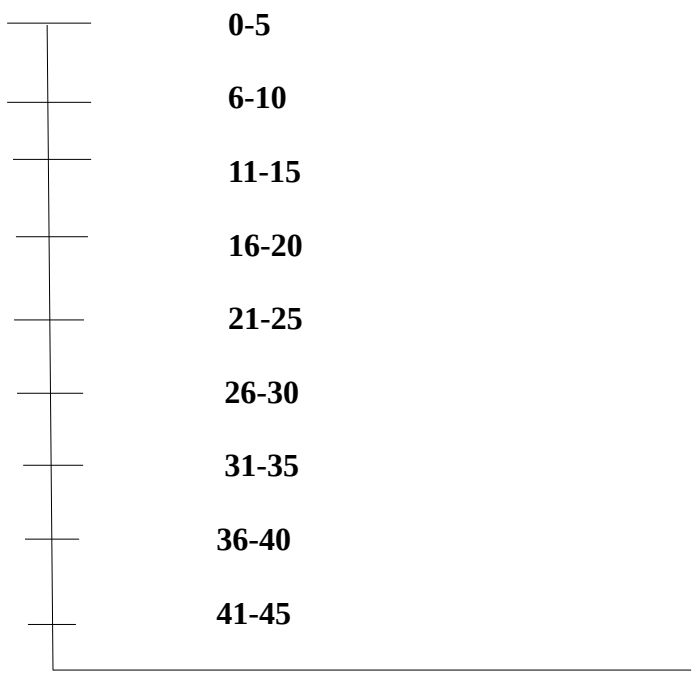
I will begin by defining the block data of 8192 {clipboard} total 40960 per packet 5 frames = 1 packet with I will create a matrix of 45 rows each with 8192 characters matrix. See chart below. I am going over the method and process defined below.



8192 * 45 rows = 368640 bits

I divide 368640 by 8192 bits and it comes up with 45 frames. I divide 45 frames by 5 = 9 packets with 5 frames per packet * 8192 byte frames in bursts of 5 equals 40960. To secure the data when sending outbound to the Internet or Intranet, I use a frame entanglement swapping frame 0 and 1. This is reassembled at the final destination or hop for old timers also this enforces endpoint to endpoint communication. I create 1 packets of 8192* 5 frames equal to 40960 I can take this further by demanding each packet is authenticated with the crypt 1300/1700 model with the created 40960 bit certificate held in memory to insure data integrity. If you wish to create an even more secure environment, The user chooses which packets order is to be sent see chart below. I could even swap the last frame’s of 44 and 45 with final packet assembly reaching the end point of communication.

Packet #	Frame sequence
1	**0-5**
2	**6-10**
3	**11-15**
4	**16-20**
5	**21-25**
6	**26-30**
7	**31-35**
8	**36-40**
9	**41-45**

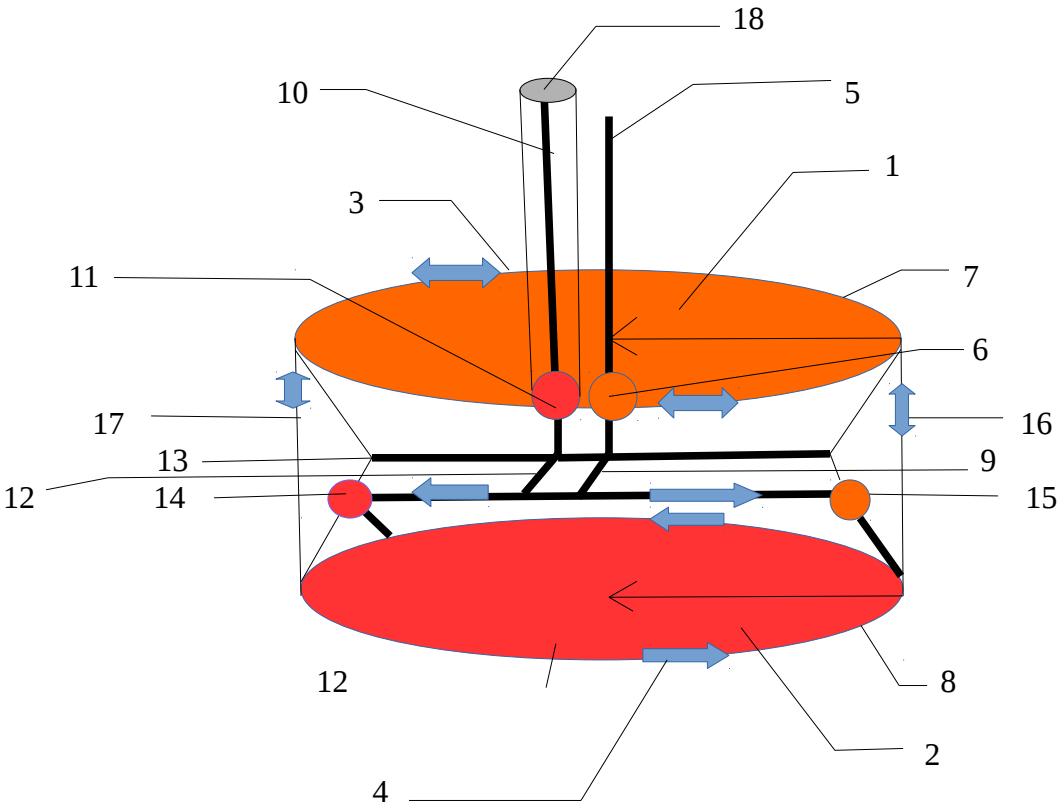


9 packets of 8192 bytes burst with frame sequences of 5. total per packet 5 * 8192= 40960.

Chapter 3

Cryptographic 1300/1700 Energy Model Design

Cryptographic 1300-1700 Energy Model Visual Design



1. Curvature Motion light Energy
2 Curvature Motion heavy energy
3. Clockwise motion 1st Dimension
4. Counter Clockwise Energy Regeneration 2nd dimension
5. 1st Data String a 4096 bits 1st Dimension
6. Gateway Check orange node point 1st dimension
7. Orange Elliptic curve 1693 Bits
8. Red Elliptic Curve 1759 Bits
9. 2nd Dimension Data String a 8192 /2 =4096 security encapsulated
10 1st Data String b 3072 Bits 2nd Dimension
11 Gateway Checkpoint 2nd Dimension
12 2nd Data String b 8192 Bits
13 1st Data Bridge Public
14 gateway Red Spectrum Check Point
15 2nd Data Bridge Private masked
16 Direct Link-1 4096 + 3072 = 7168
17 Direct Link-2 4096 + 4096 = 8192
18 Fiber Optic case with wiring String B encapsulated 8192 bits

Cryptographic 1300-1700 Energy Model Design Method and Process

I will now present a updated Cryptographic Energy Design based on Dynamic Heat and Asymmetrical Energy principles and applications. I will be discussing the method and process of this model

As you can see the energy in chart 1-B, This is a complex model and curvature is represented by shades of Orange and Red -color spectrum's. I have introduced data Bridges and two direct links.

The 1st curvature uses 1693 bits and the 2nd uses 1759 for a total of 3452 bits. Depending on the number of cycles used examples 19 and 29 I can generate 1693 * 19 = 32167 bits + 1759 * 29 = 51011 bits total bits 32167 + 51011= 83178 < 368640 The system architecture can only support 131072 bits so the number of cycles could support prime number cycles 19 and 29 also if you will notice a common number among 19 and 29 is 9 making this a common trait. To complete the processing I must now add the linear strings of the following that are supported.

1st data string a = 4096
1st data string b = 4096
2nd data string a = 3072
2nd data string b = 8192
Direct Link-1 = 7168
Direct Link-2 = 8192

data array = 83178 (elliptic) + 4096 + 4096 + 3072 + 8192+7168+8192 (linear) = 117994 this system supports this model because 117994 < 368640

The Cryptographic models are based on the Color spectrum's when crossing to dimensional space and bridges in relations to linear based strings coupled with Public and Private {masked} bridges there but not there used to authenticate and mask the IP Packet. The Elliptic colors use more heat and energy as well.

If I set up a series of arrays we could find the total number of bits based on the following example above. A pseudo program has been produced see below.

1st Curvature = a
2nd Curvature = b
1st data string = c
2nd data string =d
directlink-1 =g
directlink-2 =h
a= 32167
rem 1st curvature 1693 Prime number *19 cycles
b= 51011
rem 2nd curvature 1759 Prime Number * 29 cycles
c = 4096
d = 4096
e= 3072
f = 8192
g= 7168
h= 8192

array-1 = {a,b}
rem curvature
array-2 = {c,d,e,f}
rem data strings
array-3= {g,h}
rem direct links
array-4 = array-1 + array-2
array-4=83178+19456 = 102634 bits
array-5 = array-2 + array-3
array-5 = 4096 + 4096+3072+8192+7168+8192= 34816

This system design could support this Cryptographic model because 137450 < 368640 bits

This model uses a combination of both Linear and Curvature motion and Color spectrum Energy equating to a Cryptographic model design as discussed in previous copyrighted models this is being employed and in fact is being improved upon.

I can now subtract 368640 – 137450 and now have =231190 bits to use for my password encryption.

This model uses a combination of both Linear and Curvature motion and Color Spectrum Energy equating to a Cryptographic model design as discussed in previous copyrighted models this is being employed and in fact is being improved upon. I would like to add that because I have 231190 bits I could also create a cryptographic password that insures each IP Packet Integrity and authenticity example:

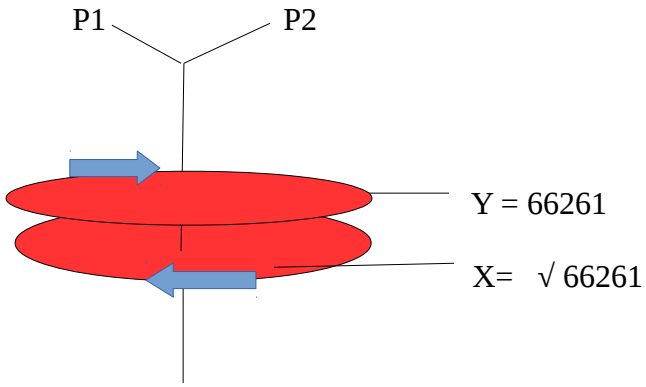
1). I can use a Data string of 2048 bits create parallel strings name it p1+ and p2- The user chooses either p1+ or p2- and than access the curvature space using a prime number of 1699 bits with 39 cycles= 66261 bits and the 2nd curvature takes the number and compresses it = 257.412120927. The next step is to add the following 2048 (linear) + 66261 (1st curvature) + 257 (2nd curvature rounded) total equals 68566 to use for password security. The Equation can be written as follows: also see below linear and curvature diagram 1-p

Z {p1 or ,P2-} = 2048 bits Linear

Y = 66261 bits= Curvature

W = (√X) + Z + Y

B1 = W/2
B2= √68566



I have created two spaces that can be used to break bits into chunks of data this creates a mechanism for multiple paths the final product is below:

B1 = 68566/2 = 34283
B2 = √68566 = 261.851102728

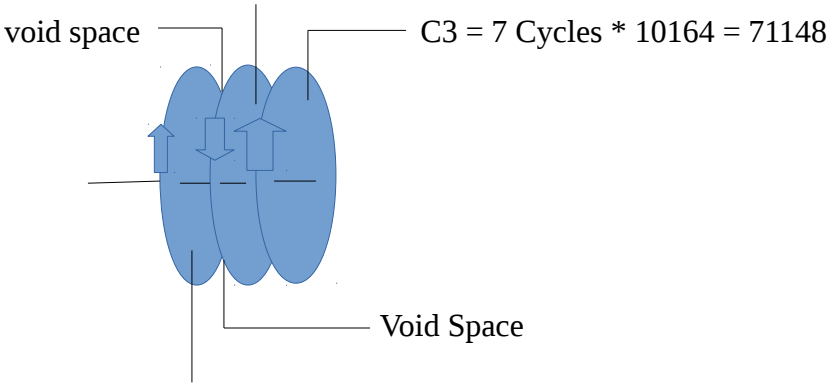
To reverse this you simply take the final product * the number being divided example:

B1 = 34283 *2 = 68566

B2 = (261.851102728) 2nd = 68565.99999987 not exact bit decay

I wanted to use a different approach to password security encryption and padding mainly the type of motion will be both linear and circular utilizing on the circular motion number of cycles while the strings use different mathematical Operations. Please view the model below: The number of bits I have for padding and encryption is 231190 – 68566 = 162624 bits

C2 = 9 Cycles * 10164 = 91476



C1 = 162624 / 16 cycles = 10164 bits

The padding scheme is not overly complex C1 = C2+ C3 = 16 = 9 +7 = 16 A balanced equation but the trick behind this is I use a data string that has access to clockwise and counter clockwise motions with C2 and C3 using cycles that are not balanced in Nature. A closer description is in order. C1 represents the 2nd dimension it supplies energy to C2 and C3 void space subatomic particles and atomic particles. The 2nd dimensional particles fill the vacuum in the to C2 and C3 while at the same time energy is being used and expanded in the second dimension. Thus the rate of expansion when using a constant is not based on one event but multiple events on a time line this is understood under Irwin Schroedinger work and his principles.

c1 can be stated using two mathematical operations using two events with 1 variable or time line.

Event 1 Event 2

C1 = (√x2)2nd power = C2 + C3 The rate of expansion in C1 > C2 or C3 or in this model 16 > 9 or 16 > 7.

You may ask about X2 and where does this energy come from. This is derived by the fact that X2 does not recognize our time and space 1st dimension thus energy is infinite within the 2nd dimension because of non recognizable time and space from the 1st dimension. The idea that 8∏r2G is not valid here because of using multiple events to create a time line and using 16 cycles that exceeded gravity binding particles that excel past void null space or the 1st dimension. The Scientist who supported this are mainly Nobel Peace Prize Scientist and are recognized as the best of minds but it does not appear that their theories are correct. This needed to be addressed and sometimes simple Equations can be translated into complex theories such as Einstein's Equation or Stephen Hawkins singular black hole event and Horizon I applied the same principle in using a simple equation and creating a complex theory and has been balanced as such.

If you take the speed of light roughly at 186,000 * 2 =372,000. The design I am presenting pushes 368640. If we divide this 368640 / 372000 = 0.990967742= 1- 0.990967742= 0.009032258 This shows a fractional decay discreet but it is shown almost 1% not quiet making this design a very efficient and effective design.

Final Thoughts

Chapter 4

I have improved upon my CPU Model by adding layered models for CPU 1, CPU1-3 supports 36 layers Red spectrum and CPU 4 supports 9 layers for a total of 45 layers 368640 bits the CPU's can support. The memory now supports 368640 bits establishing equilibrium . The CPU and Memory uses fiber optic wires encased to promote privacy, speed, and security. This model is updated to include color spectrum's that load hardware configuration based on the color spectrum matching CMOS to CPU for Hardware configuration. I have also included in this design terminator blocks, 8 pin wires, along with a double bladed fan system 24 star topology, buffer chips to prevent I/O overflows along with terminator switch blocks.

This project involved making improvements on prior existing designs along with modifications. I also created a password and padding algorithm for this project. I created a simple equation that discusses multiple event horizons along with complex theory.

The Video card has been updated to provide a stronger level of privacy and security using the New Crypt 1300-1700 model along with the introduction of a 40960 bit hardware certificate for authentication and password security also employs dual bladed fans 24 point star configuration and using two elliptic circles using clockwise and counter clockwise motion coupled with a linear data string,

The 1300-1700 model employs three dimensional geometric shapes using dynamic linear strings, dual curvature blocks, and two direct interfaces also employs a dual color spectrum bridge with the red using fiber optic wiring and encapsulation of data also I have created a built in ROM certificate with principles of Dynamic Energy being deployed. I have reached the end of the line with this cryptographic Model without making serious a serious overhaul of this design.

I have deployed Fiber Optic wiring on the CPU ,Memory and other components allowing me to both excel past the speed of light 186,000 in terms of bits 368640 bits in this design. I will begin to process and represent bits on a micro level commonly named nanobits in future designs. Please note with the implementation of Fiber Optics on most major components the capability of processing bits, bytes, addresses, frames within the Internal structure of this design will far exceed the External structures capable of reaching at the speed of light.

As stated earlier this year, I intended to make a design that was greater than > 100,000 bits. This has been completed . \ Met 2019 goal.

If you wish to view more work, Please visit my website below

www.barrysscientificbasedproducts.info

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10/07/2019

Barry L. Crouse