# System 32768 Interface Design

**By**

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## Introduction

Welcome to my scientific based work entitled Barrys system 32768 Interface design. The purpose of this work is to provide support for existing Computer Motherboards that process less than or equal to 32768 bits are are data intensive along with system bottle necks that are present.

1). Some of the features of this design are it has three adapters that can be connected with the other motherboards processing 32768 bits * 3 = 98304 bits on this board it self.

2). The Dual System fans come with dual blades in a 24 star configuration to insure the interface is not overheating quickly do to intensive bit processing.

3). The on board Fiber Optic memory chips carry eight fiber optic wires total bits 8192 per chip and 4 chips total 32768 bits utilizing linear and Curvature motion with the ability to process between five and 11 Cycles in the BIOS (see screen for memory configuration) also the deployment of gateway and node point switches off and on allow the ability to process faster by Intelligent Design Paths.

4). The private adapter has four area spaces or nodes assigned a class C private reserver address of 192.168.1.x with intergrated encrypted MAC and Authentication processes.

5). The IP Geo locater is a dual based chip requiring the new authentication method and process and or agreement before information is sent or received a way of verifying information.

6). Reserved space or buffer chip has been added on this design to avoid bottle necks and intensive system I/O's.

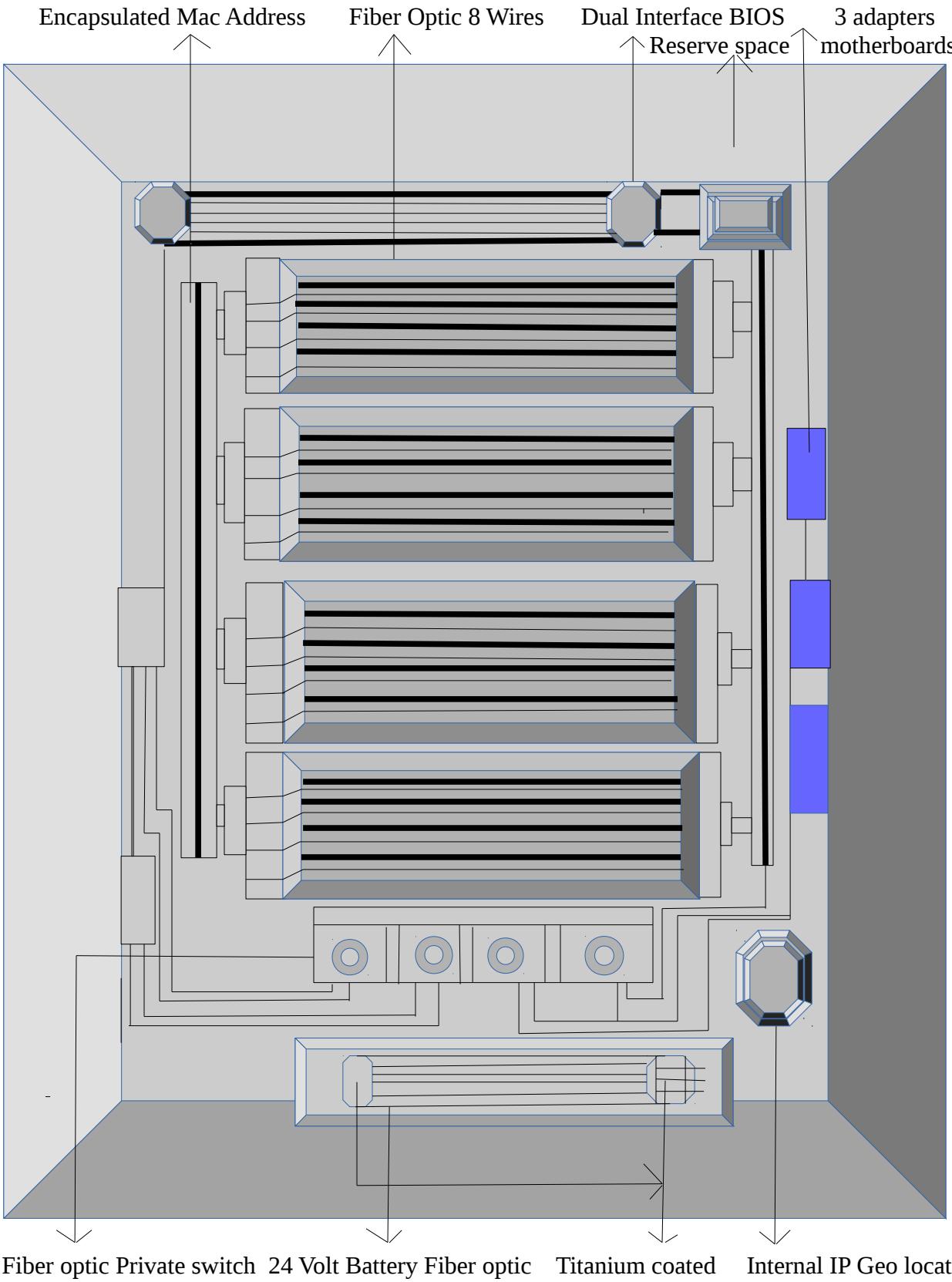
7). BIOS Date information is encrypted to avoid Zombie Relay Stations.

8). A unique Authentication process has been designed for this Interface for extra security measures and is used for the Private encrypted mac address.

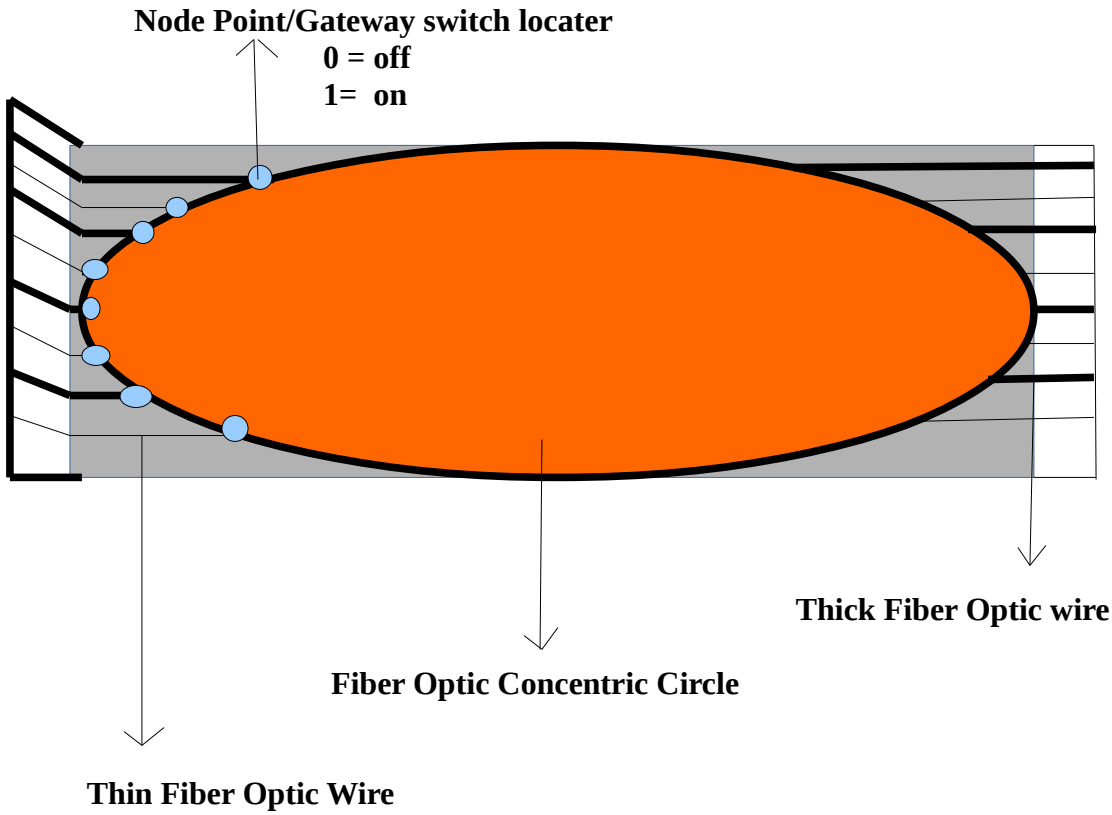
9). I have also added a new method to encrypt Private address mac addresses.

## Table of Contents

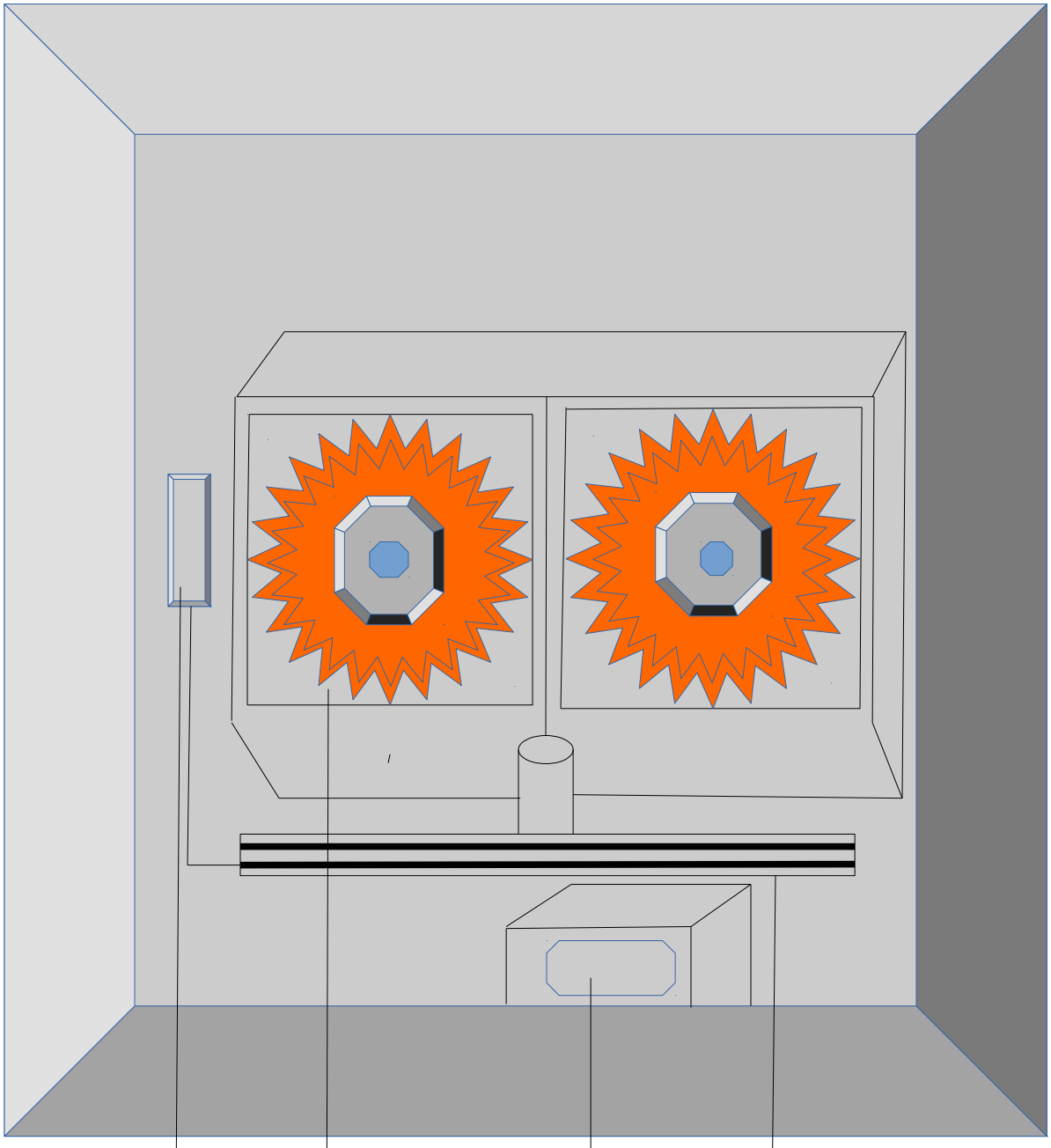
**System 32768 Interface Design – Top View Figure 1-A**



**Memory Chip Back View 2-A**



**System 32768 Interface Design Rear View Figure 3-A**



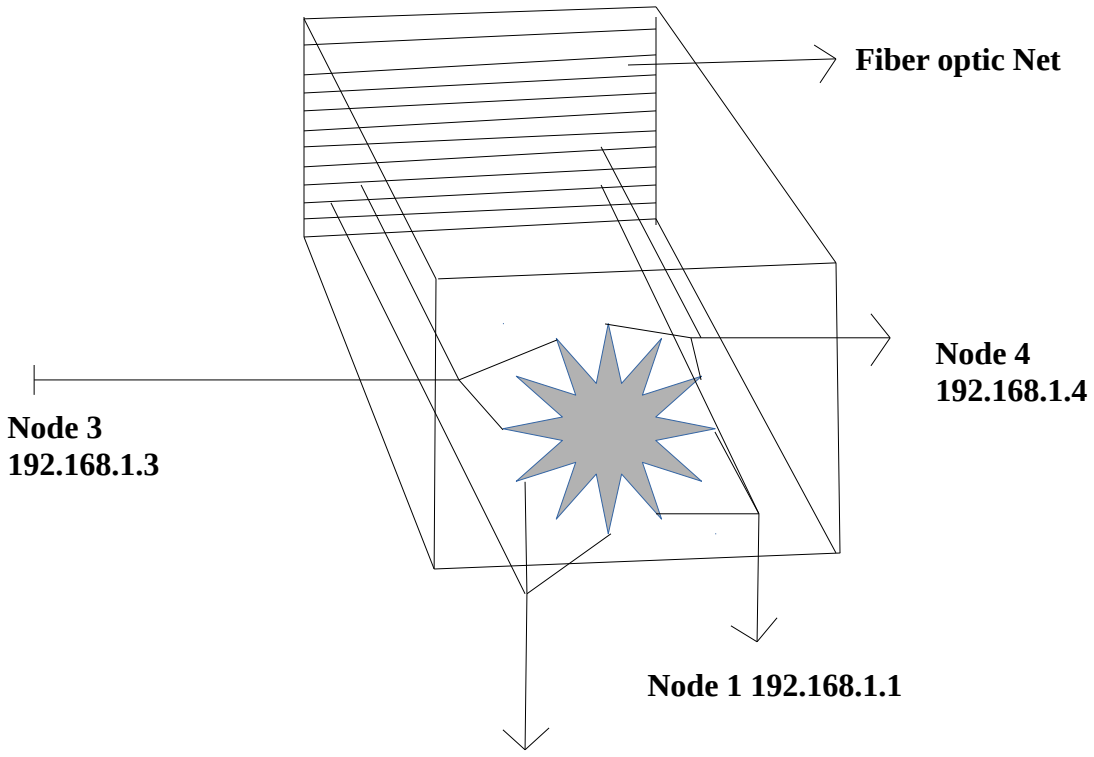
**Private Raid Adapter**

**Dual Titanium Interface Fan**

**Dual Encapsulated Fiber Optic**

**Internal Fan Interface BIOS**

**Perspective View of Private Adapters 4-A**




| Node 1 | Area of Space | Encrypted MAC Address |
|---|---|---|
| 192.168.1.1 | 1 | 16 Character Field see Chapter 2 |
| 192.168.1.2 | 2 | 16 Character Field see Chapter 2 |
| 192.168.1.3 | 3 | 16 Character Field see Chapter 2 |
| 192.168.1.4 | 4 | 16 Character Field see Chapter 2 |

# Chapter 2

# Overview of the System Bus Design

I will now provide some more detailed information about this system bus design.

1). The mac addresses are encapsulated and or enclosed to provide better security for IP packet formation with the ability to process 8192 bits per memory chip I have the ability to expand the MAC address from 12 characters with six fields to 16 characters with eight fields example below:

**a). F0: B4: C7: D9: E5 : G7 Standard Field 6**

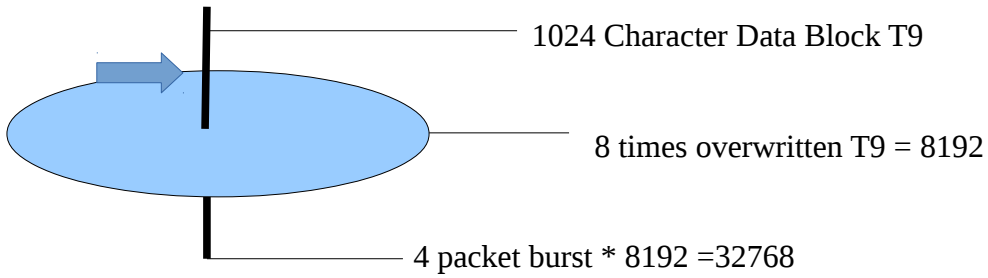
**b) F0: B6: C9: D5: E3: Z8 : L5 : T6 Expanded field 8**

The expansion of the system bus design can now be applied to Internal Class C Private addresses example I wish to use node Point 1 in Area 1 with a assignment of 192.168.1.1(see chapter 1) I now have the ability to expand the MAC address assignments to 8 fields instead of the standard 6 fields to further complete this I would have to clone this address

**F0: B6: C9: D5: E3: Z8 : L5 : T6 Real Address**

**F0: B6: C9: D5: E5: Z8 : L5 : T9 Cloned Address**

The next step is to write over the Cloned address with a block of data each address example T9 is given a 1024 block of data and is written over 8 times to get to the 8192 data block. This can be further developed by sending 4 packet bursts of 8192 data blocks to achieve 32768, but the main idea in this work is to show to extend a product's life cycle.



1).I can now use the built-in Authentication key to validate the Internal packets and send it out to the outside world little humor. The Authentication key is in the next chapter.

2). I have created a reserve space chip with three areas of space total 6 terrabytes of Data to hold data in Que temporary to avoid bottle necks because if the system bus has the ability to connect to three boards of 32768 bits it will be necessary to hold data in Que in some instances.

3).The dual system Fan has a configuration of a 24 star topology allowing the system bus board to cool down quickly because of the amount of bits being processed.

4). I have allowed for 4 memory chips with 8 wires on each chip at 1024 bits total 8192 bits 3 volts =1024 bits so 12 volts are required.

5). The system bus board has the ability to access 4 private Class C addresses making it dynamic in nature when assignment for a packet is needed based on Intelligent Design path or metrics.

6). A dual BIOS has been implemented to provide integrity check of hardware and configuration of system bus to the motherboard itself also included is system integration.

7). The memory chips use fiber optic wiring that are encased and or encapsulated this allows for address processing to be quickly completed free from signal and broadcast interference.

I have provided a brief overview of this design with specifications and now will proceed to the next chapter password and Authentication keys.

# Chapter 3

# Password and Authentication keys

BIOS Password Length 16384 Bits Field Specs

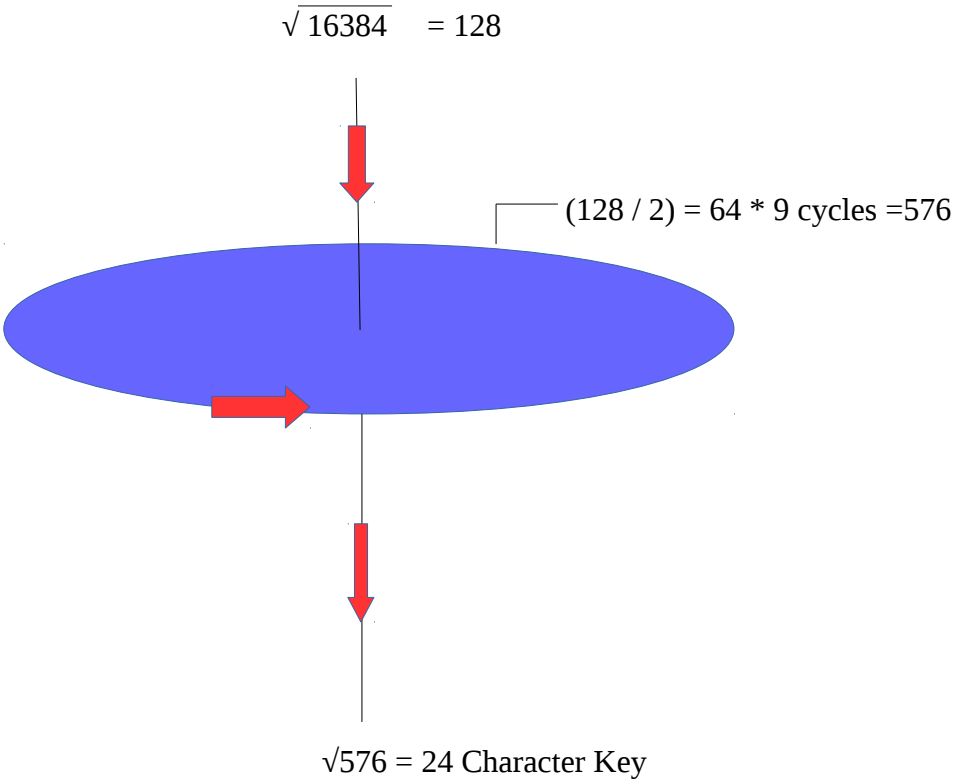
16384 Bits Total
16 Character Mac Field
1 Character = 1024 bits 16 * 1024
√1024 = 32 + {0,1}

The Password to enter the BIOS has a total Bit Strength of 16384 represented by 16 characters and translated into 1 character = 1024 bits this is compresses to 32 using a 0 as off and 1 as on making a total of compressed characters 33 {32 + 1 } or { 32 + 0 } . The reason why this is set to 16384 bits instead of 32768 bits is to allow for backward compatibility. On another note, I left legacy based Password systems intact 12 characters in length. The only thing is you would have to create 12288 bits with no compression to adapt to this system sample below:

Legacy Based Bit Password Length

12288 Bits total
12 characters total length
1 Character = 1024 12 * 1024
No compression for security

**Authentication Process**




The Authentication key uses a unique process above by completing the following :

1). The square root of 16384 on the clip board is square rooted and this come out to 128 Linear
2). The next step is to take 128/2 = 64 * 9 cycles = 576 Curvature
3). Finally ,The 576 is than square rooted and the key is represented by 24 characters encrypted. Linear.

This process is unique to this interface only and would not work with other systems. This also represents a Unique system interface process only for this design another security feature. The spatial motion is Linear, Curvature, and than Linear. In a password process the normal range in length is between eight to 16 Characters in this process it is represented by a 24 character key to authenticate and communicate to the adapters that have systems wishing to communicate to it.

# Chapter 4

# BIOS Screens

**Barrys Scientific Based products Interface Screen**

**Password Entry **************  **Date ** / ** / ******

1). **Memory Chip Configuration**

2). **BIOS Configuration and Internal Check Authentication**

3). **Reserve Space Configuration**

4). **Private Adapter Configuration**

5). **IP Geo Locater Authentication Check**

6). **Return to Main Menu**

**Barrys Scientific Based Products Interface Screen**

**Memory Chip Configuration**

**1). Standard Bit Processing 4096 total 16384 bits**

**2). Optimal Bit Processing 8192 total 32768 bits**

**3). Standard Mac Address 6 fields**

**4). Optimal Mac Address 8 fields**

**5). Fiber Optic Memory Address Processing 32768 * 5 cycles = 163840 bits per second**

**6). Fiber Optic Memory Address Processing 16384 * 11 cycles = 180224 bits per second**

**7). Return to Main Menu**

**Barrys Scientific Based products Interface Screen**

**BIOS Configuration and Internal Check Authentication**

**1). CMOS 1 Primary**

**2). CMOS 2 Secondary**

**3). CMOS 1 Secondary**

**4). CMOS 2 Primary**

**5). CMOS 1 Internal Authentication Check**

**6). CMOS 2 Internal Authentication Check**

**7). Return to Main Menu**

**Barrys Scientific Based products Interface Screen**

**Reserve Space Configuration**

| | | | | |
|---|---|---|---|---|
| **1).** | **Reserve Area Space 1** | **0 – 2 Terra bytes** | **0 = no** | **1 = yes** |
| **2).** | **Reserve Area Space 2** | **0 – 2 Terra bytes** | **0 =no** | **1 = yes** |
| **3).** | **Reserve Area Space 3** | **0 – 2 Terra bytes** | **0 =no** | **1= yes** |
| **4).** | **Return to Main Menu** | | | |

**Barrys Scientific Based products Interface Screen**

**1). IP / MAC Address Adapter 1**

**2). IP/ MAC Address Adapter 2**

**3). IP/ Mac Address Adapter 3**

**4). Return to main Menu**

I would now like to turn your attention to the Date on the main menu on the BIOS Screen this has been encrypted to avoid some cyber attacks and attempting to gain control of the Interface creating a Zombie Relay Station. The Date is encrypted as follows

Characters in each Date field example **/ is represented by 4 characters per star example January could be shown as 01 but represented by a AaZGF4H9. The characters can be represented by setting up a table  see example below

0 = AaZG
1 = F4H9

This is setup in a background process . The password process used in Chapter 3 using 32768 can be used in the Date screen in the BIOS.

I will now provide my final thoughts in the next chapter.

# Chapter 5

# Final Thoughts

This interface design software wise is unique in many ways it has a distinctive password, authentication process, system bus with mac addresses and BIOS screens that allow for dynamic changes based on system needs.

The hardware also has a distinctive design by using a cooling process for allowance of high intensity bit processing. A reserved chip is added to this design for placing I/O's in temporary storage to avoid additional system bottlenecks. A dual BIOS has been added and is reflected on BIOS Screens.

1). Motion usage combines linear and curvature hardware and software which combines gateway and node points along with authentication processes.

2). The Date Filed uses a unique process to prevent Zombie relay stations that go undetected by other operating systems.

3). The Authentication process can be integrated with the encrypted MAC Address for a unique method and process and will see future developed and implemented on more advanced system designs.

4). A new method to encrypt a MAC address to a Private Class C address has been introduced for further Product development in future Designs.

The introduction of this system interface allows for Previous Motherboard Designs too have a extended product life cycle because of the backward compatibility of the BIOS and updated hardware configuration also with the introduction of a new authentication method and process I am able to apply this model in principle on more advanced system designs.

I have answered the question about taking a product that was past it's life cycle and extending it with enhancements Authentication and Encrypted MAC addresses. Yes , it can be done.

Thank you for you time and viewing this work ! If you wish to view further works, Please goto my website below:

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