

**Barrys SS-125 Motherboard Design 4<sup>th</sup> Generation**

by

**Barry L. Crouse**



BARRYS SCIENTIFIC BASED  
PRODUCTS

IT PRODUCT DESIGN

## Introduction

I would like to take the time in Thanking each and everyone of you for reading this Science and technology based work. I have made improvements on the SS-110 Motherboard Design please view the following below:

- a). Data Strings 4 strings per chip 4096 bits per string total 8 strings total 16384 per chip total bits 131072
- b). Tri Core CPU CPU 1 (12 layers), CPU 2 (11 layers) CPU (9 layers) asymmetrical total bits **131072**.
- c). Tri CMOS with color spectrum to match CPU Processor's
- d). New Cryptographic Energy Model Multiple Path Processing
- e). 8 bridge wiring scheme 8192 bits memory chip
- f). **8192 Bit CPU Pin Grid array**
- g). Deployment of 8192 bits used for clipboard migrating away from 4096 bits

1). The Visual **Model Super Sonic 125 Motherboard 1-A General View** overall view of the product and demonstrates a Industrial Design because of it's unique characteristics. The detailed features that are within the Design accompanies in views 1-a through 10-A with detailed specs. The features of this design comes with Asymmetrical three intertwined CPU's that have 12 layers, 11 layers and 9 layers total bits **131072** along with color spectrum's to interface with various components example is CMOS uses alternative path choices. This CPU Asymmetrical Design now has the ability to use 8192 bits instead of the standard 4096 bits to the clipboard. The memory chip has 8 wires for the Data bridges to push through the wires 8192 bits establishing equilibrium between the CPU and Memory.

2). **Patent Ideal 2 Method and Single 131072 Data Block processing**. This is discussed as a method and process of Internal Packet exchanges within the Motherboard Design itself and is upgraded as well.

3). **Patent Idea New Cryptographic Energy Model Design-Crypt 1300-1700 model**. This is shown as an Industrial Design along with the method and process. This comes with dynamic bit data strings, linear and dual curvature elliptic circles with password encryption and padding Mathematical equation with process, method and dynamic heat via color now added is port redirects with certificate validation using linear and Elliptic Kinetic Energy.

4). I have updated the Video card and slot that now supports the Crypt 1300-1700 model with no more PKCS 12.

5). I have updated some components on the Motherboard to use a ring Do Decagon Star Network Topology Design including the video Card, adapters, and fans.

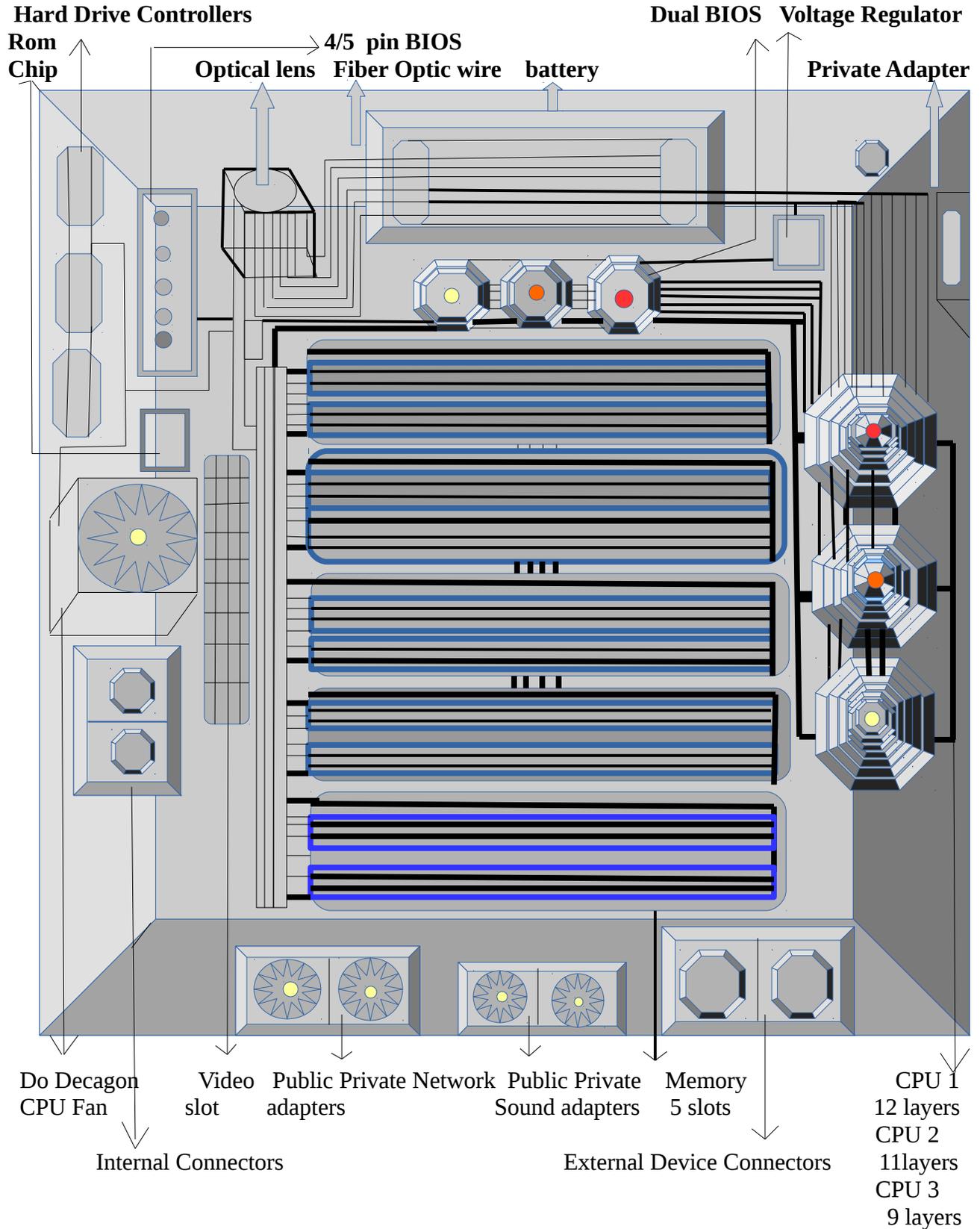
6). Built in Hardware Certificate now includes the Crypt 1300-1700 Model.

**This is a 4th generation motherboard Design.** Once again thank you for reading this work !

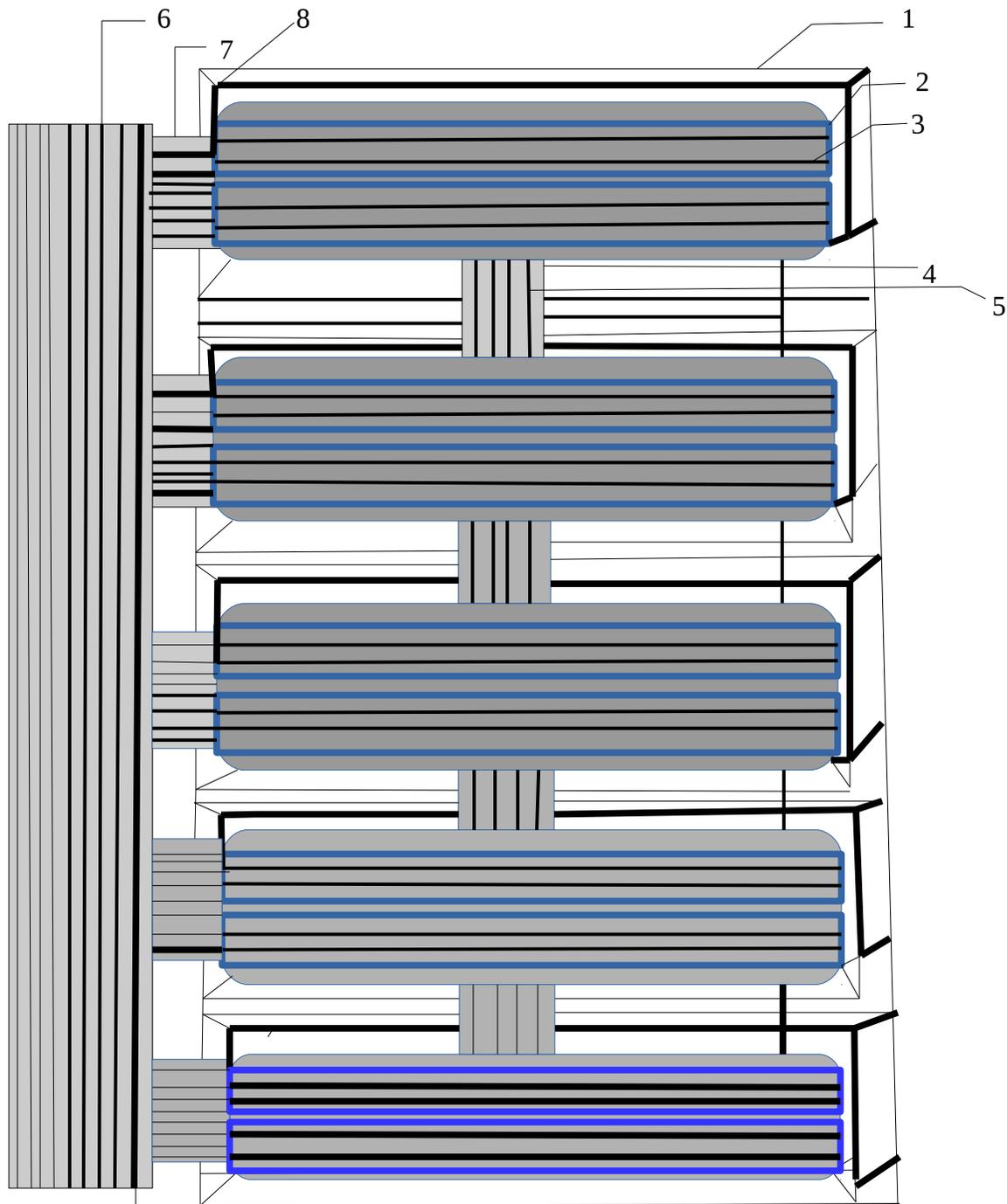
## **Table of Contents**

- 1). **Visual Design**
- 2). **131072 Data Block processing**
- 3). **Cryptographic 1300/1700 Energy Model Design**
- 4). **Final Thoughts**

**Model Super Sonic 125 Motherboard- Design 1-A General View**

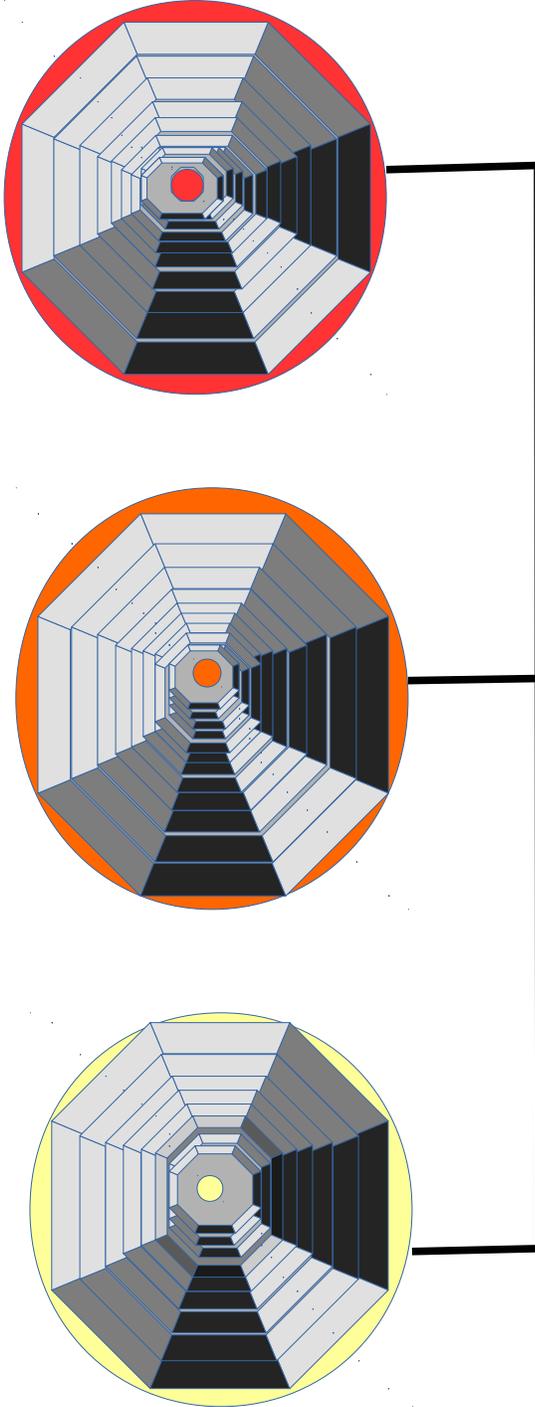


## Model Super Sonic 125 Dual memory Core General View 2-A



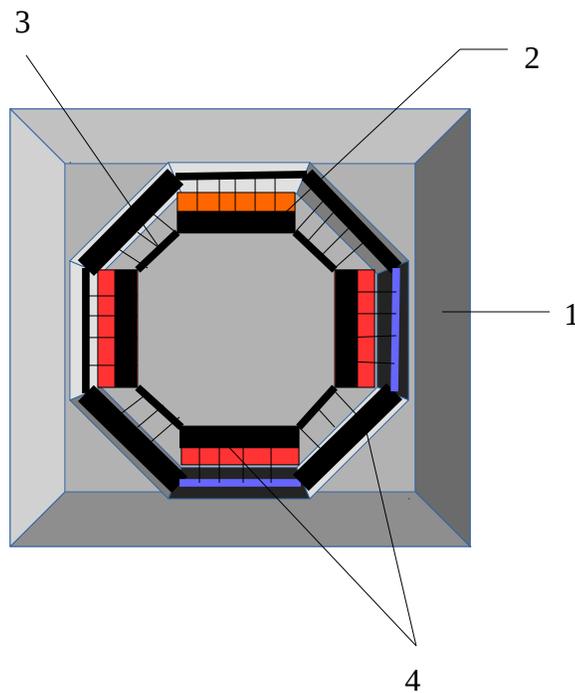
- 1). Fitting to hold Memory Chips
- 2). Banks 4 banks per Dual Core memory chip 20 banks total
- 3). Data Strings 4 strings per chip 4096 bits per string total 8 strings total 16384 per chip total bits 131072
- 4). Area Memory Bridge (Bytes to Frames switches)
- 5). 8 data strings per bridge 2048 bits per wire total 16384 bits
- 6). Fiber Optic tube address encasement 5 wires
- 7). Address Bridge 8 wires 8192 bits per wire to process Fiber Optic
- 8). Dual Core Memory Chips

## Model Super Sonic 125 CPU and Topology Design General Views



- 1). CPU 1 Layers 1-12 Red Color Spectrum
- 2). CPU 2 Layers 1-11 Orange Color Spectrum
- 3). CPU 3 Layers 1-9 Yellow Color Spectrum

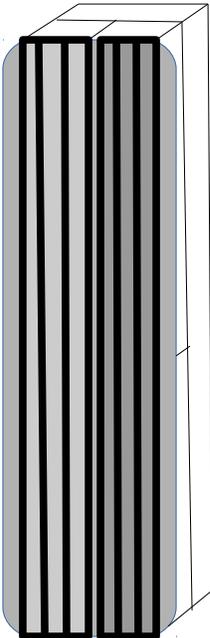
## Model Super Sonic 125 CPU Octagon 8192 Pin Block Array



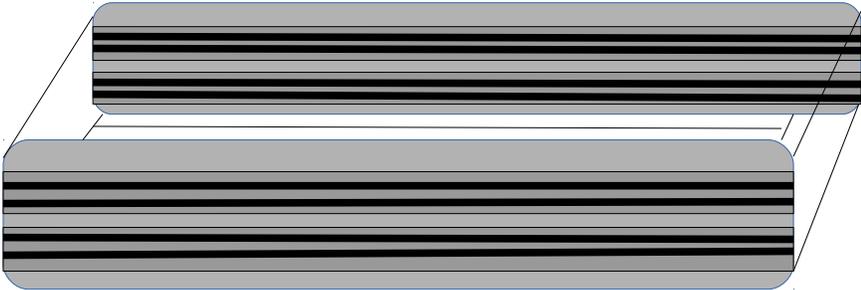
- 1) CPU Fitting
- 2). Pins into the CPU Fitting 4 Sets =4096 bits
- 3). Pins out to the CPU Fitting 4 Sets = 4096 bits
- 4). CPU total Pins into and out into CPU 8192 bits

**Model Super Sonic 125 Motherboard memory Front and Side View 2-A**

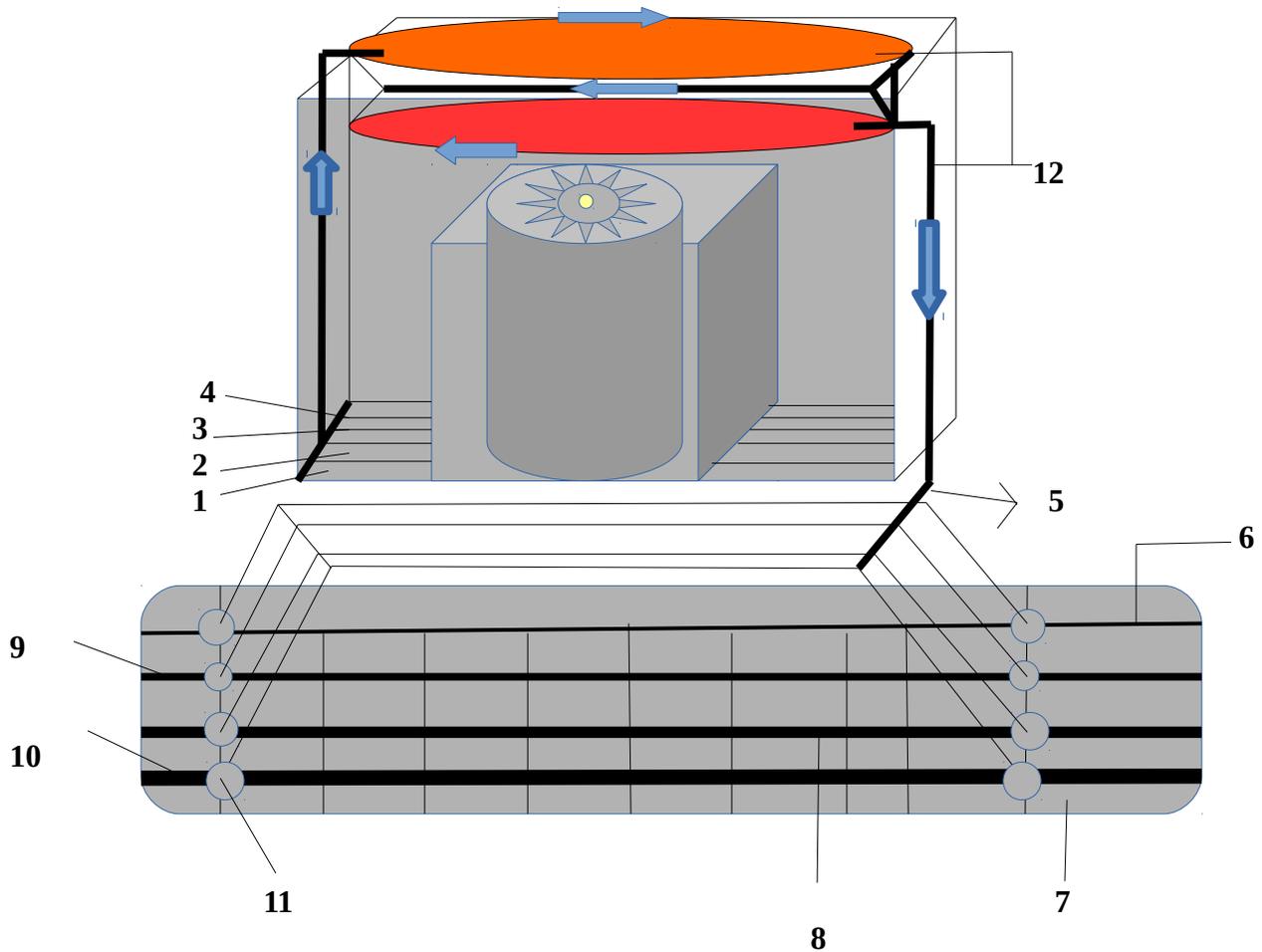
**Dual Core**



Dual Core Memory Front View

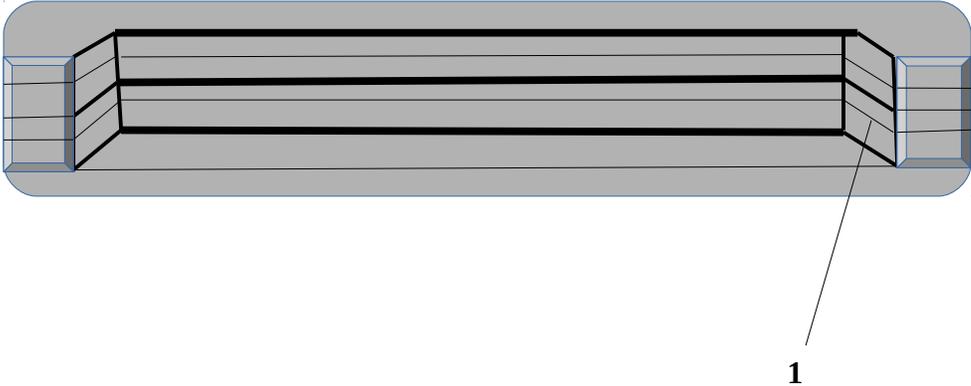


## Model Super Sonic 125 Industrial Video /Fan Idea 4- A General View



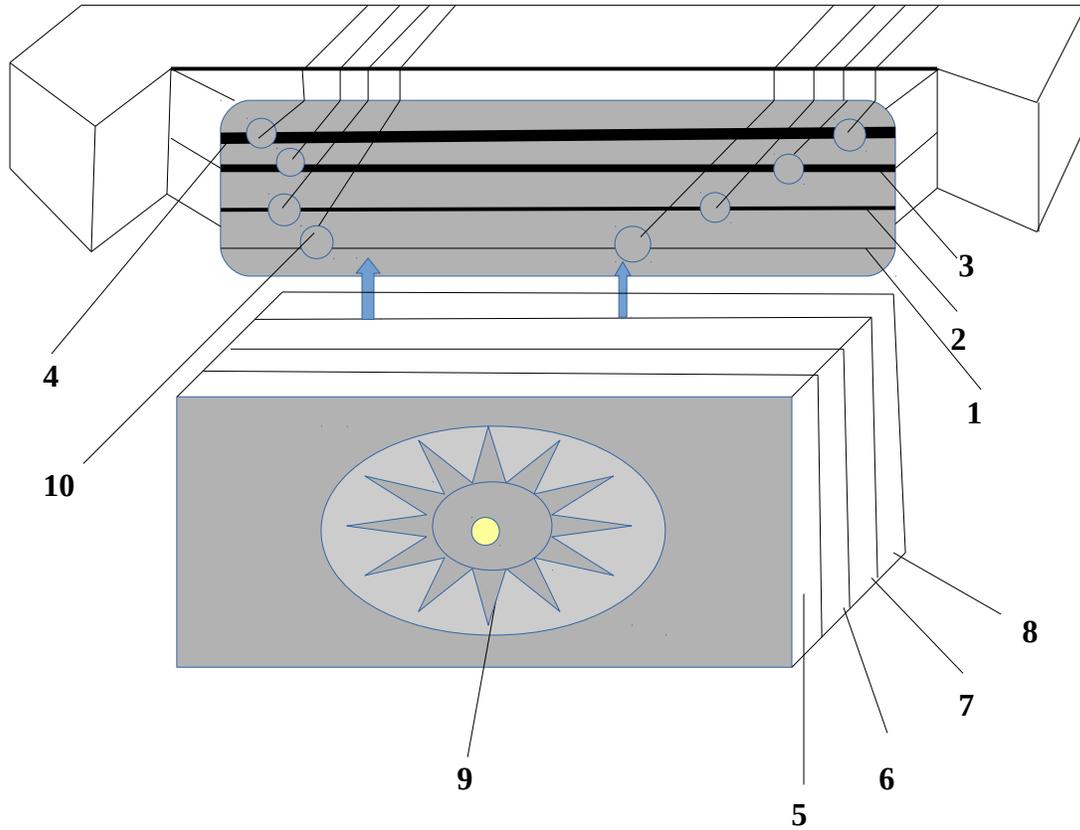
- 1). Public Video Area Crypt 1300-1700 model
- 2). Private Video Area Crypt 1300-1700 Model
- 3). Shared Video Area Crypt 1300-1700 Model
- 4). Reserved Video Area Crypt 1300-1700 Model
- 5). Video Data Bride 4 slots
- 6). Public Data String
- 7). Titanium video fitting
- 8). Shared Data String
- 9). Private Data String
- 10). Reserved Data String
- 11). Node Points (End to End point connection)
- 12). Crypt 1300-1700 Model energy regeneration

**Model Super Sonic 125 Industrial Patent video slot 5-A General View**



**1) Side view of the slot where the Video Card is placed.**

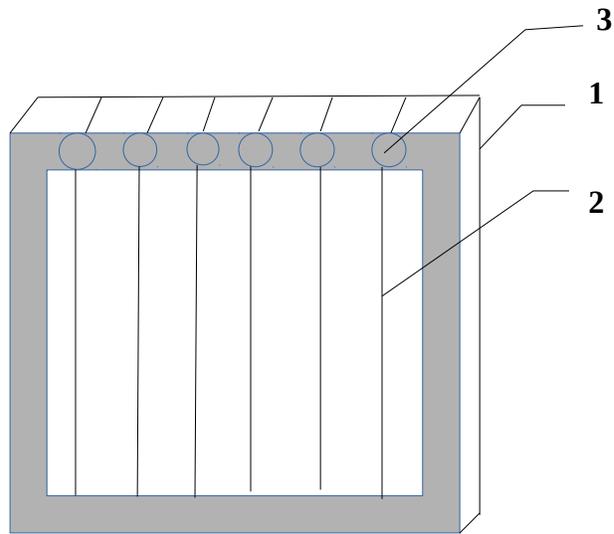
## Model Super Sonic 125 Industrial Video slot specs Idea 6-A General View



- 1        **Public Data String Crypt 1300-1700 Model**
- 2        **Private Data String Crypt 1300-1700 Model**
- 3        **Shared Data String Crypt 1300-1700 Model**
- 4        **Reserved Data String Crypt 1300-1700 Model**
- 5        **Public Video Slot**
- 6        **Private Video Slot**
- 7        **Shared Video Slot**
- 8        **Reserved Video Slot**
- 9        **Video Fan**
- 10       **Node Points**

## Model Super Sonic 125 Industrial Idea 7-A General View

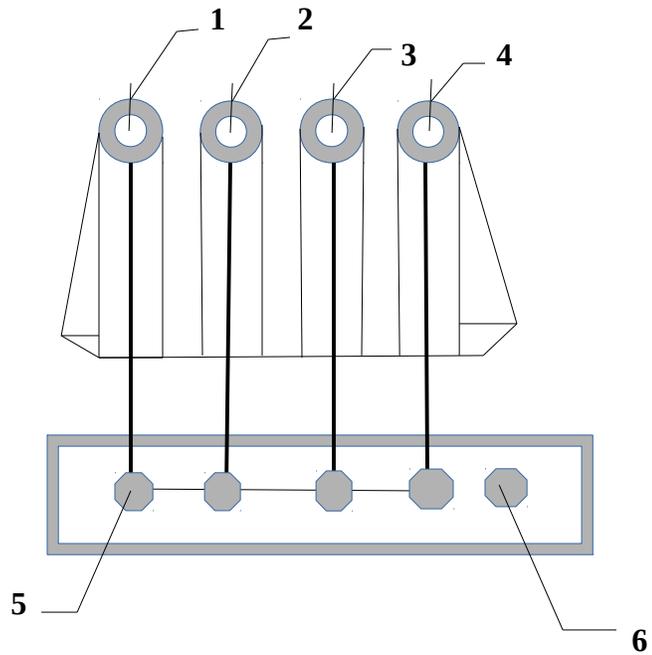
### Voltage Regulator 5 wire Check



- 1). Overall view of chip
- 2). 6 wires inside chip to check flow of voltage 1024 bits per wire total 6144 bits
- 3). Node Point check testing wires for on and off conditions

## Model Super Sonic 125Industrial BIOS Idea 8-A General View

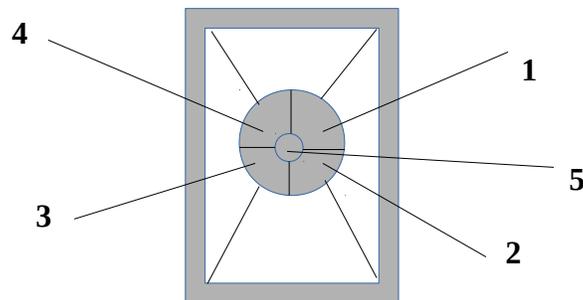
### 4/5 Pins BIOS



- 1). Public BIOS Pin
- 2). Private BIOS Pin
- 3). Shared BIOS Pin
- 4). Reserved BIOS Pin
- 5). BIOS Bins that connect to node Points
- 6). BIOS Pin Clearing areas of spaces

## **Model Super Sonic 125 Industrial ROM Chip Idea 9-A General View**

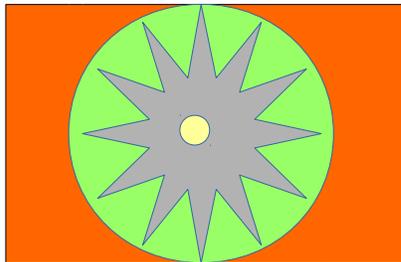
### **Encrypted -Crypt 1300-1700 Model Built in Certificate ROM Chip**



- 1). Public Area of Space**
- 2). Private Area of Space**
- 3). Shared Area of Space**
- 4). Reserved Area of Space**
- 5). Certificate on burned on platter read only**

## **Model Super Sonic 125 Industrial Rom Chip specs Idea 10-A General View**

### **Barrys Scientific Based Products Encrypted -Crypt 1300-1700 Model**

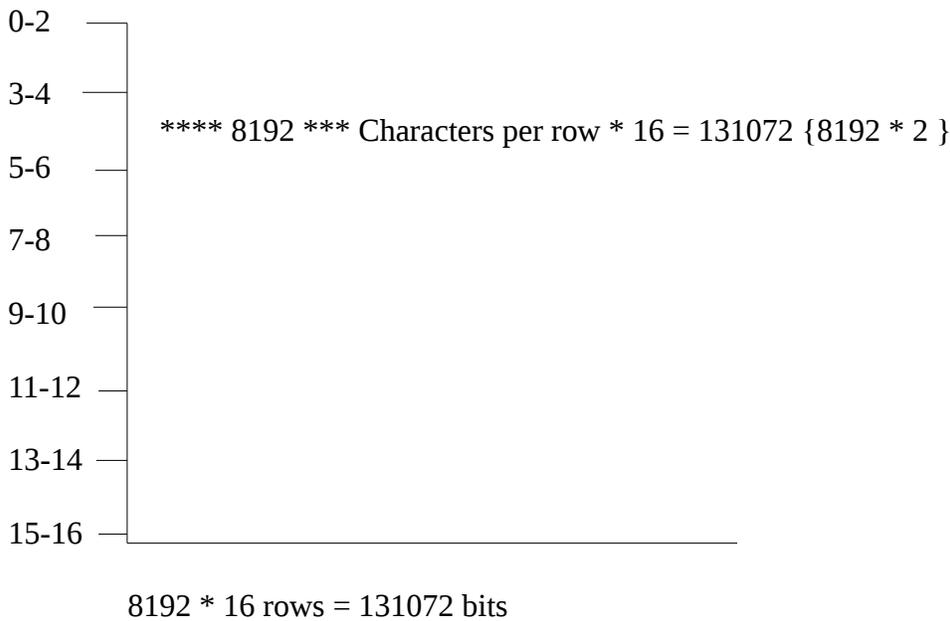


This Certificate is used to check for authenticated Hardware updates it is built into the motherboard via ROM Chip to access the Certificate which is capable of 30383 must use the Crypt 1300-1700 Model

## **Chapter 2**

### **Single 131072 Data Block processing**

I will begin by defining the block data of 8192 {clipboard} total 16384 per packet with I will create a matrix of 16 rows each with 16384 characters matrix. See chart below. I am going over the method and process defined below.



I divide 131072 by 8192 bits and it comes up with 16 frames. I divide 16 frames by 2 = 8 packets with 2 frames per packet \* 8192 byte frames in bursts equals 16384. To secure the data when sending outbound to the Internet or Intranet, I use a frame entanglement swapping frame 0 and 1. This is reassembled at the final destination or hop for old timers also this enforces endpoint to endpoint communication. I create 8 packets of 8192 byte frames equal to 131072 I can take this further by demanding each packet is authenticated with the crypt 1300/1700 model with the created 30383 bit certificate held in memory to insure data integrity. If you wish to create an even more secure environment, The user chooses which packets order is to be sent see chart below. I could even swap the last frame's of 15 and 16 with final packet assembly reaching the end point of communication.

Packet #	Frame sequence
1	1-2
2	3-4
3	5-6
4	7-8
5	9-10
6	11-12
7	13-14
8	15-16

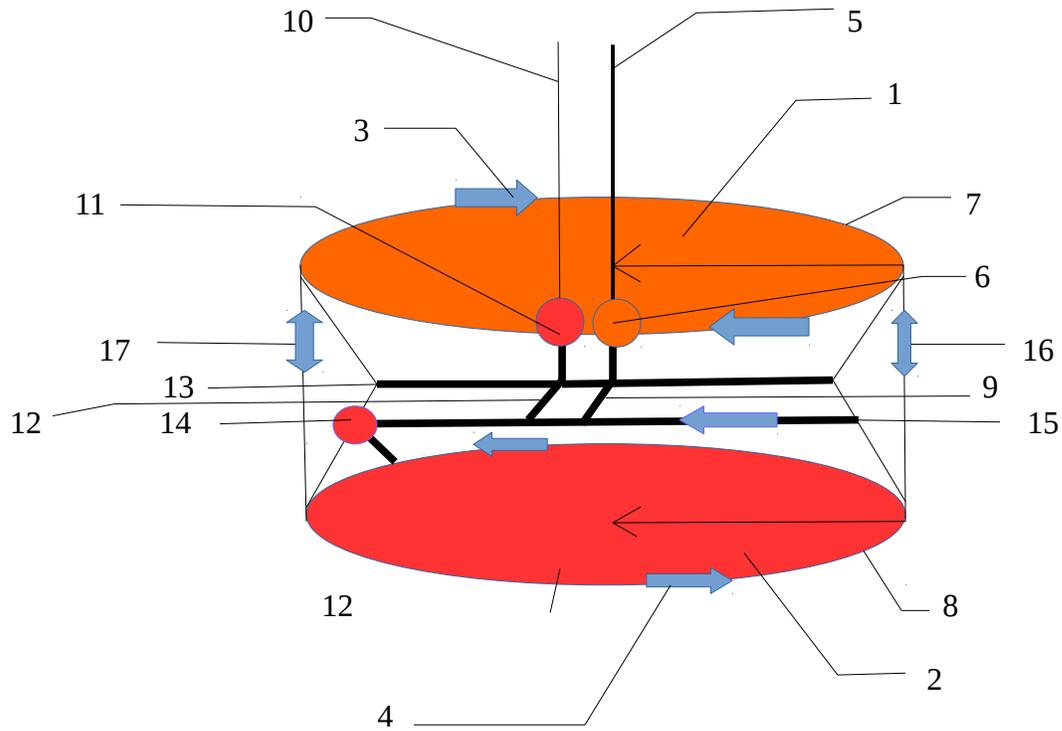
**8 packets of 8192 bytes burst with frame sequences of 2. total per packet  $2 * 8192 = 16384$ .**

**1).  $131072 / 16 = 8192$  per two frames/per packet of 8 bursts**

## **Chapter 3**

### **Cryptographic 1300/1700 Energy Model Design**

## Cryptographic 1300-1700 Energy Model Visual Design



1. Curvature Motion light Energy
2. Curvature Motion heavy energy
3. Clockwise motion 1<sup>st</sup> Dimension
4. Counter Clockwise Energy Regeneration 2<sup>nd</sup> dimension
5. 1<sup>st</sup> Data String a 2048 bits 1<sup>st</sup> Dimension
6. Gateway Check node point 1<sup>st</sup> dimension
7. Orange Elliptic curve 1301 Bits
8. Red Elliptic Curve 1511 Bits
9. 2<sup>nd</sup> Data String a 2048 Bits
10. 1<sup>st</sup> Data String b 2560 Bits 2<sup>nd</sup> Dimension
11. Gateway Checkpoint 2<sup>nd</sup> Dimension
12. 2<sup>nd</sup> Data String b 3072 Bits
13. 1<sup>st</sup> Data Bridge Public
14. gateway Check Point
15. 2<sup>nd</sup> Data Bridge Private masked
16. Direct Link-1  $2048 + 2560 = 4608$
17. Direct Link-2  $2048 + 3072 = 5120$

## Cryptographic 1300-1700 Energy Model Design Method and Process

I will now present a New Cryptographic Energy Design based on Dynamic Heat and Asymmetrical Energy principles and applications. I will be discussing the method and process of this model

As you can see the energy in chart 1-B, This is a complex model and curvature is represented by shades of Orange and Red -color spectrum's. I have introduced data Bridges and two direct links.

The 1<sup>st</sup> curvature uses 1301 bits and the 2<sup>nd</sup> uses 1511 for a total of 2812 bits. Depending on the number of cycles used examples 17 and 19 I can generate  $1301 * 17 = 22117$  bits +  $1511 * 19 = 28709$  bits total bits  $22117 + 28709 = 50826 < 131072$  The system architecture can only support 131072 bits so the number of cycles could support asymmetrical cycles 17 and 19. To complete the processing I must now add the linear strings of the following that are supported.

1<sup>st</sup> data string a = 2048  
1<sup>st</sup> data string b = 2560  
2<sup>nd</sup> data string a = 2048  
2<sup>nd</sup> data string b = 3072  
Direct Link-1 = 4608  
Direct Link-2 = 5120

data array =  $50826$  (elliptic) +  $2048 + 2560 + 2048 + 3072 + 4608 + 5120$  (linear) =  $70282$  this system supports this model because  $70282 < 131072$

The Cryptographic models are based on the Color spectrum's when crossing to dimensional space and bridges in relations to linear based strings coupled with Public and Private {masked} bridges there but not there used to authenticate and mask the IP Packet. The Elliptic colors use more heat and energy as well.

If I set up a series of arrays we could find the total number of bits based on the following example above

1<sup>st</sup> Curvature = a  
2<sup>nd</sup> Curvature = b  
1<sup>st</sup> data string = c  
2<sup>nd</sup> data string = d  
directlink-1 = g  
directlink-2 = h  
a = 22117  
rem 1<sup>st</sup> curvature  $1301 * 17$  cycles

b= 28709  
rem 2<sup>nd</sup> curvature 1511 \* 19 cycles  
c = 2048  
d = 2560  
e= 2048  
f = 3072  
g= 4608  
h= 5120

array-1 = {a,b}  
rem curvature  
array-2 = {c,d,e,f}  
rem data strings  
array-3= {g,h}  
rem direct links  
array-4 = array-1 + array-2  
array-4=22117+28709 = 50826 bits  
array-5 = array-2 + array-3  
array-5 = 2048 + 2560+2048+3072+4608+5120=19456

This system design could support this Cryptographic model because  $70282 < 131072$  bits

This model uses a combination of both Linear and Curvature motion and Color spectrum Energy equating to a Cryptographic model design as discussed in previous copyrighted models this is being employed and in fact is being improved upon.

I can now subtract  $131072 - 70282$  and now have =60790 bits to use for my password encryption.

This model uses a combination of both Linear and Curvature motion and Color Spectrum Energy equating to a Cryptographic model design as discussed in previous copyrighted models this is being employed and in fact is being improved upon. I would like to add that because I have 60790 bits I could also create a cryptographic password that insures each IP Packet Integrity and authenticity example:

1). I can use a Data string of 1024 bits create parallel strings name it p1+ and p2- The user chooses either p1+ or p2- and than access the curvature space using a prime number of 1321 bits with 20 cycles= 30383 bits. The next step is to add the 1024 bits = 31407 bits to use for password security. The Equation can be written as follows: also see below linear and curvature diagram 1-p

$Z \{p1 \text{ or } ,P2-\} = 1024 \text{ bits Linear}$

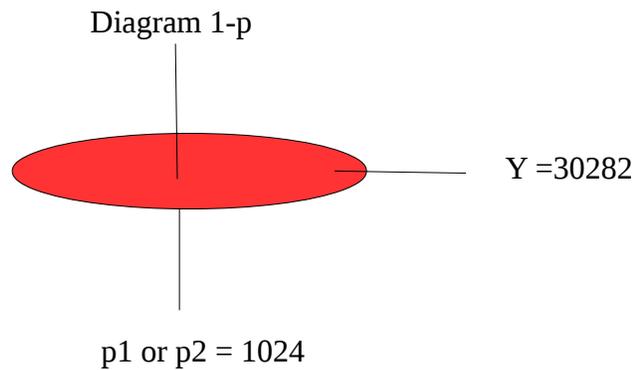
$Y = 30282 \text{ bits} = \text{Curvature}$

$W = Z + Y$

$B = W/3$

$B = W/19$

$B = W/29$



I have created three spaces that can be used to break bits into chunks of data this creates a mechanism for multiple paths the final product is below:

$$B = 31407/3 = 10469$$

$$B = 31407/19 = 1653$$

$$B = 31407/29 = 1083$$

To reverse this you simply take the final product \* the number being divided example:

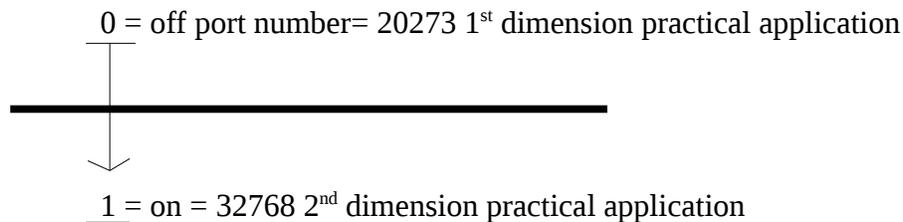
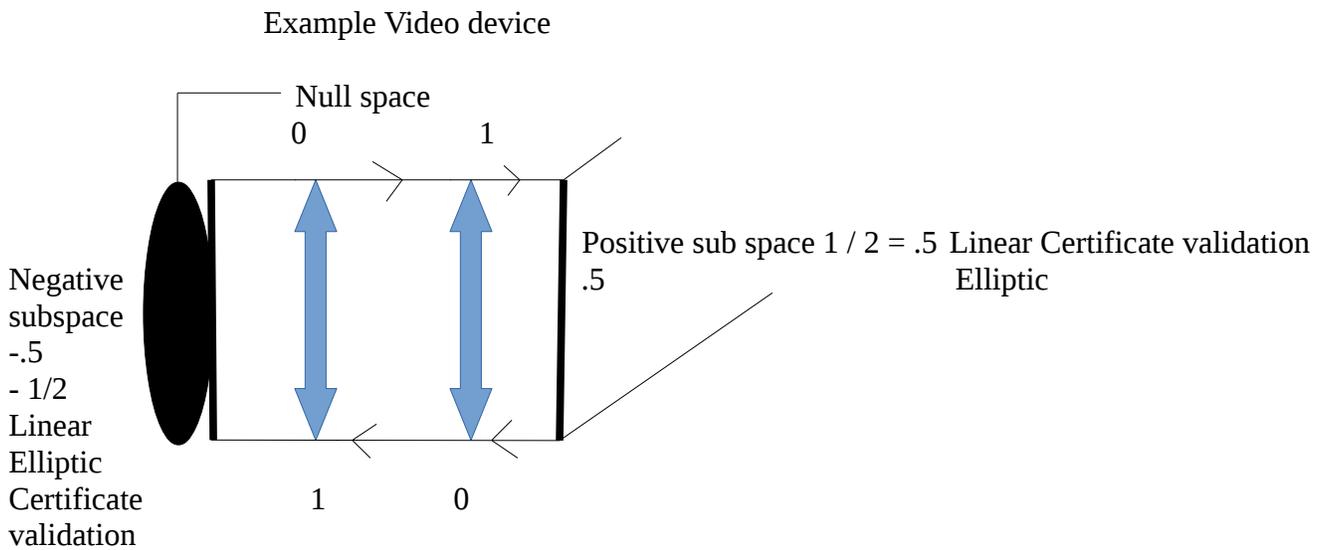
$$10469 * 3 = 31407$$

If you will notice, I have  $60790 - 31407 = 29383$  bits left over, This needs to be utilized and how this can be used is by padding the password encryption with the spare bits. This can be achieved by the following:

$$60790 - 31407 = 29383 \text{ bits}$$

$$B = 60790/1 = 31407 + 29383 \text{ Bits}$$

$B = 29383/2 = \{14691 + 1\}$  1st subscript +  $\{14692+0\}$  2nd subscript total = 29383 . Thus I have created a double subscript for password and padding a IP packet that needs protection. If I want to add extra protection for each subscript simply compress both scripts. If you will notice in the 1<sup>st</sup> and 2<sup>nd</sup> subscript, I can create a binary switch “0 = off” and “1=on” to turn password and padding on or off for this particular design for better data protection at users discretion. This can be further expanded to include 4 conditions see visual Picture and table below.



## Testing conditions

- 1) 0 = off 1= on port number 20100
- 2) 1 = on 0 = off port number 20273
- 3) .5 = subspace of 1 binary switch off dimensional space is positive port switch redirected to port 32768 with positive area of space
- 4) -.5= subspace of 0 binary switch is off dimensional space is negative port switch redirected to “null space” void” space.

The purpose of adding two additional testing conditions are the following:

- 1). Create fractional time space see numbers 3 and 4.
- 2). Creates a fractional time space where the switch is in the off position but creating positive energy **item number 3** is off but has a fractional time space or 2<sup>nd</sup> dimensional space of on positive energy.
  - a). example I have switch off = 0 but really in the on position 1 so  $0 | 1| + 2^{\text{nd}}$  dimension positive
- 3). Creates a fractional Space where the switch is in the off position but creates negative energy see **item number 4** is in the binary switch position of off but has a fractional time space or 2<sup>nd</sup> dimensional space of negative energy.
  - b). example I have a switch off = 0 but really in the on position 1 so  $0 | 1| - 2^{\text{nd}}$  dimension space

This creates a way to test for fractional time space also in consideration a practical application is to turn the switch off on the port number and have it redirected to a port switch in the on position. The negative space is given a “null space” . Please notice the kinetic energy in the graph 2<sup>nd</sup> dimensional spacing linear and curvature. This opens the door utilizing authenticating port numbers with linear and circular certificates for validation purposes.

The next item to be discussed is the password process please see below:

{14690+1 = 14691  $\sqrt{\quad}$  = 121.206435473 1<sup>st</sup> subscript the 2<sup>nd</sup> subscript 14692+0 =  $\sqrt{14692}$ = 121.210560596 I have compressed both of these because of the principles of asymmetry not balanced form of energy and discreet energy numbers with the deciding factor belonging to the binary switch off and on hidden variable principle, theory, and application.

The equation could be written as such ( $\sqrt{a \text{ and or } b}$ ) = d

I will now write my final thoughts on this Projects

## **Final Thoughts**

### **Chapter 4**

I have improved upon my CPU Model by adding layered models for CPU 1, CPU 2, and CPU 3 that are asymmetrical in nature CPU's supports 12,11 and 9 layers for a total of 131072 bits the CPU's can support. The memory now supports 131072 bits establishing equilibrium . This model is updated to include color spectrum's that load hardware configuration based on the color spectrum matching CMOS to CPU for Hardware configuration. I have also introduced a Pin Grid Array that processes 8192 bits and uses a 8192 Clipboard migrating away from standard 4096 bit clipboards

This project involved making improvements on prior existing designs along with modifications. I also created a password algorithm for this project along with padding also created subscripts used for padding the address spaces creating a extra layer of IP packet protection along with password protection.

The Video card has been updated to provide a stronger level of privacy and security using the New Crypt 1300-1700 model along with the introduction of a 30383 bit hardware certificate for authentication and password security

The 1300-1700 model employs three dimensional geometric shapes using dynamic linear strings, dual curvature blocks, and two direct interfaces also employs a masked bridge also I have created a built in 30383 ROM certificate with principles of Dynamic Energy being deployed.

This project was very enjoyable to see the development of a experimental Design taking shape in more ways than one !.

As stated earlier this year, I intended to make a design that was greater than > 100,000 bits. This has been completed . ✓ Met 2019 goal.

If you wish to view more work, Please visit my website below

[www.barryscientificbasedproducts.info](http://www.barryscientificbasedproducts.info)

Email [crouseb395@gmail.com](mailto:crouseb395@gmail.com)

4/17/2019

Barry L. Crouse