Barrys SS-110 Motherboard Design 4th Generation

by

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Introduction

I would like to take the time in Thanking each and everyone of you for reading this Science and technology based work. I have made improvements on the SS-95 Motherboard Design please view the following below:

a). Dual Core memory chip 5 banks 81920 bits
b). Dual Core CPU CPU 1 (10 layers), CPU 2 (5 layers) asymmetrical total 61440
c). Dual BIOS fault tolerance ,Integrity, throughput 3 wires
d). New Geometric Design Do Decagon Polygon for Fans on board
e). Buffer chip to hold bits for processing CPU and Memory.

1). The Visual **Model Super Sonic 110 Motherboard 1-A General View** overall view of the product and demonstrates a Industrial Design because of it's unique characteristics. The detailed features that are within the Design accompanies in views 2-a through 9-A with detailed specs. The features of this design comes with Asymmetrical CPU's that have 10 layers and five layers along with alternative path choices. The CPU processes up to 61440 and the memory chip 81920 with a buffer chip holding 20480 in Que. I have now added additional thin wire with now 4 thin wires.

2). **Patent Ideal 2 Method and Single 61440 Data Block processing. T**his is discussed as a method and process of Internal Packet exchanges within the Motherboard Design itself and is upgraded as well.

3). **Patent Idea New Cryptographic Energy Model Design.** This is shown as an Industrial Design along with the method and process. This comes with dynamic bit data strings, linear and dual curvature elliptic circles with password encryption and padding Mathematical equation with process, method and dynamic heat via color now added is port redirects with certificate validation using linear and Elliptic Kinetic Energy.

4). I have updated the Video card and slot with 4 areas of space using PKCS 12 security for each area of space key and sub key promoting security and privacy when viewing within the structure of this IT hardware motherboard.

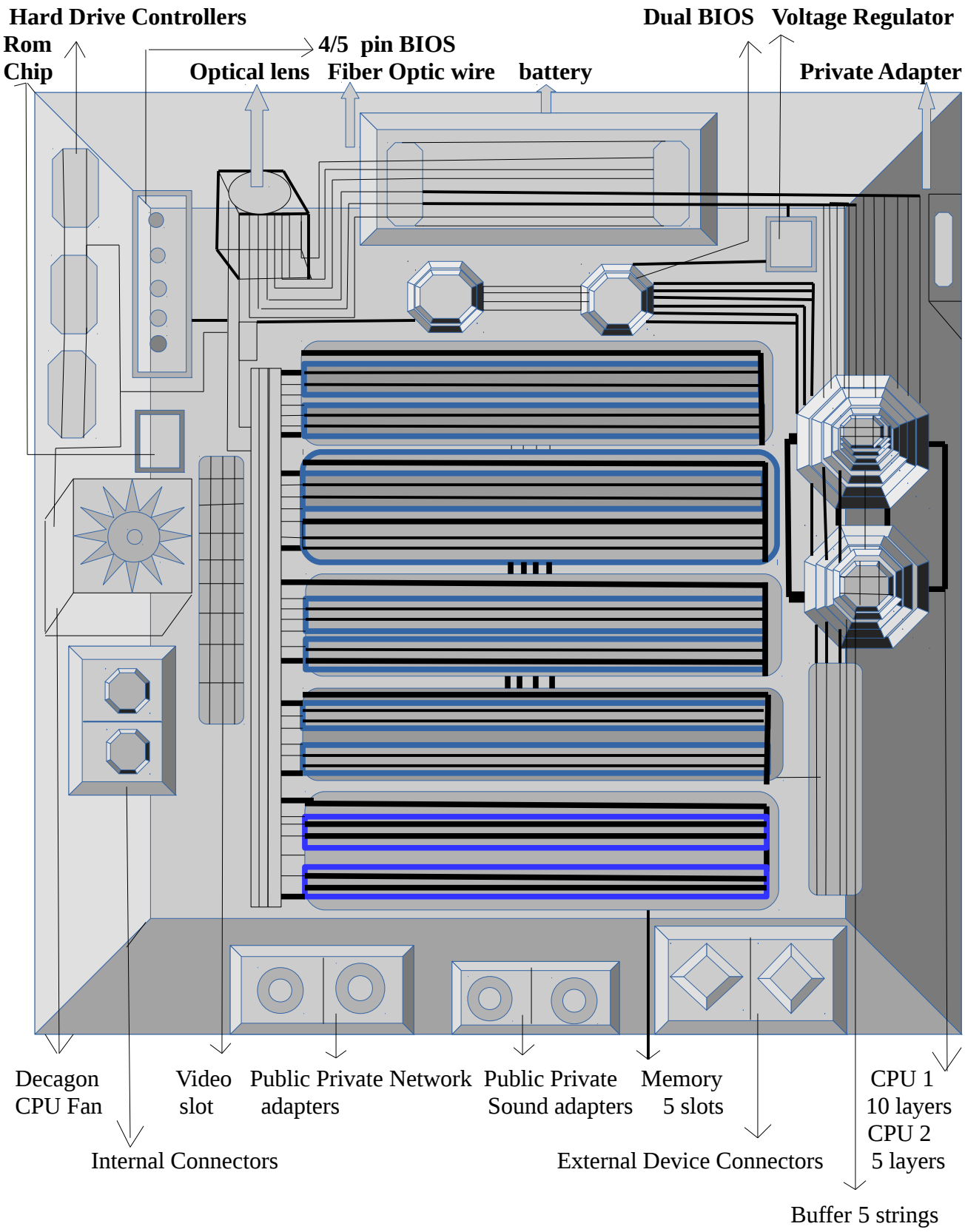
a). PKCS 12 = 1 area of space 12288 bits = 4 areas of space * 12288 = 49152 total bits

This is a 4th generation motherboard Design. Once again thank you for reading this work !

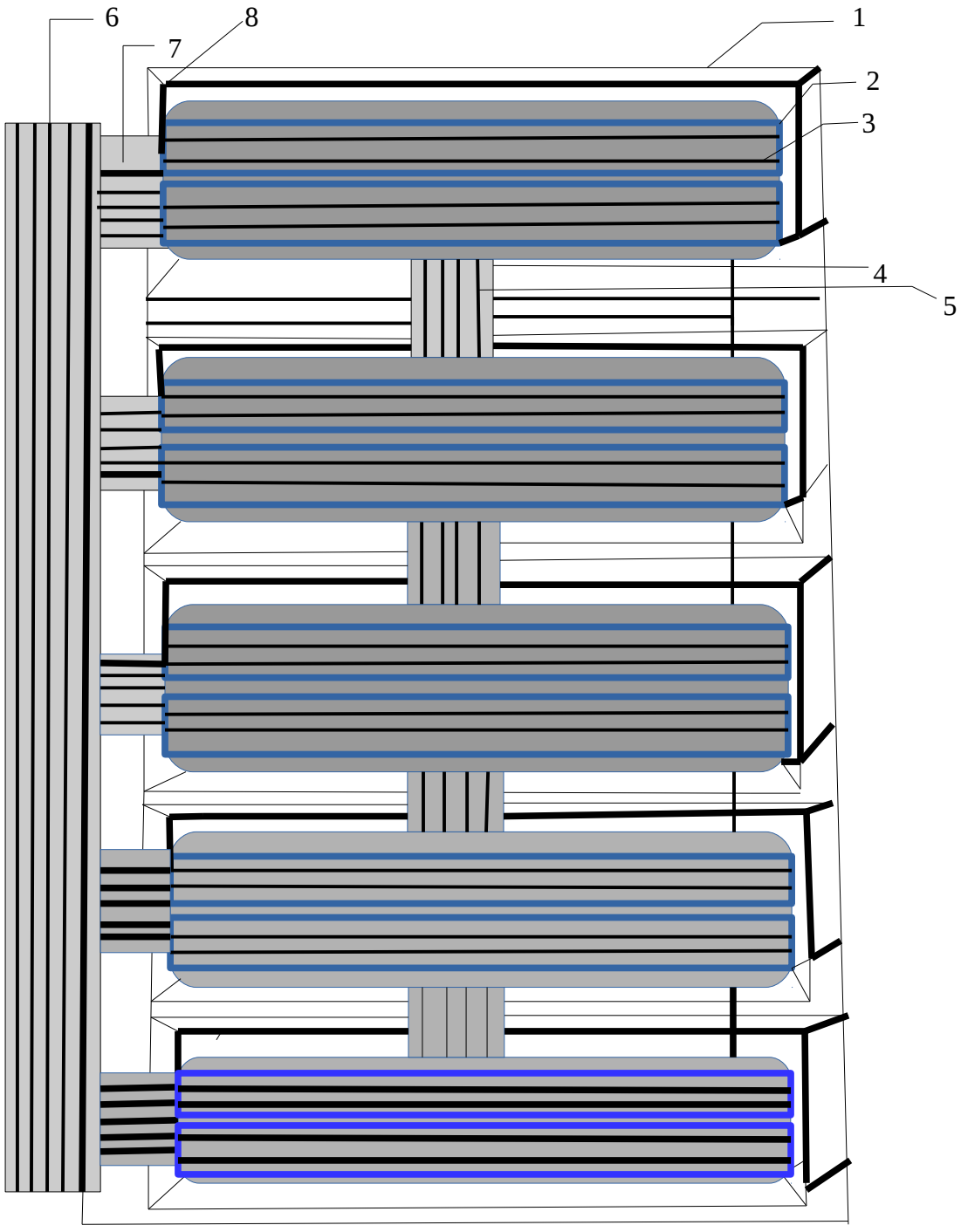
5). Fans used on the motherboard use a do decagon 12 star topology Network design increasing the ability to control the system climate better.

Table of Contents

Model Super Sonic 110 Motherboard- Design 1-A General View

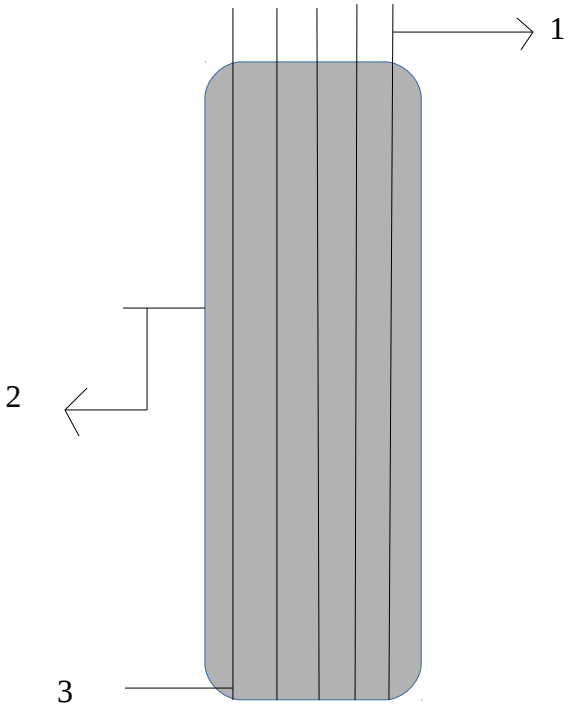


Model Super Sonic 110 Dual memory Core General View 2-A



1). Fitting to hold Memory Chips
2). Banks 4 banks per Dual Core memory chip total 10 4096 per bank total 8192 bit addressing scheme
3). Data Strings 4 strings per Bank 4096 bits per string total 20 strings per chip 81920 bit addressing
4). Area Memory Bridge (Bytes to Frames switches)
5). 4 data strings per bridge 1024 bits per wire total 4096 bits
6). Fiber Optic tube address encasement 5 wires
7). Address Bridge 5 wires 5120 bits per wire to process Fiber Optic
8). Dual Core Memory Chips

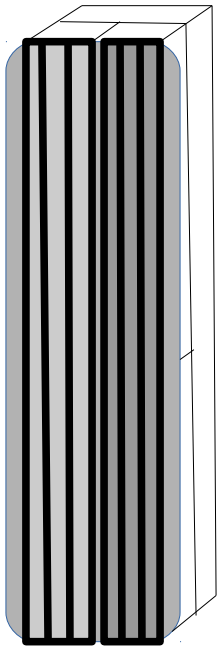
Model Super Sonic 110 Buffer memory Chip General View 3-A



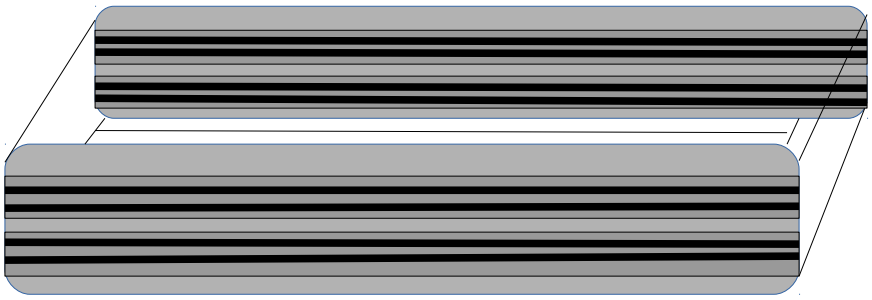
1). Wires to CPU
2). Wire to memory
3). 5 wires 4096 per wire total 20480 bit buffer chip used for queuing.

Model Super Sonic 110 Motherboard memory Front and Side View 2-A

Dual Core

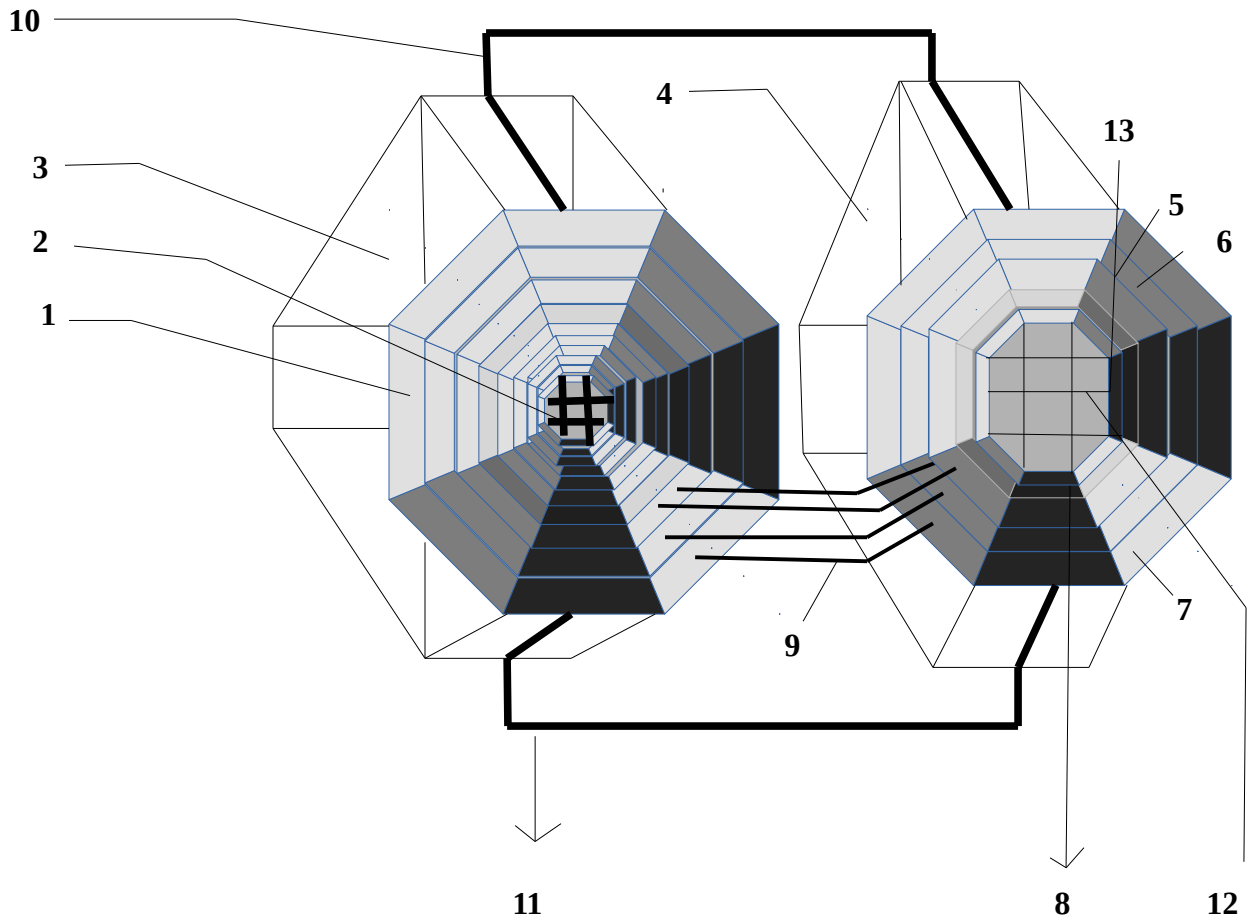


Dual Core Memory Front View



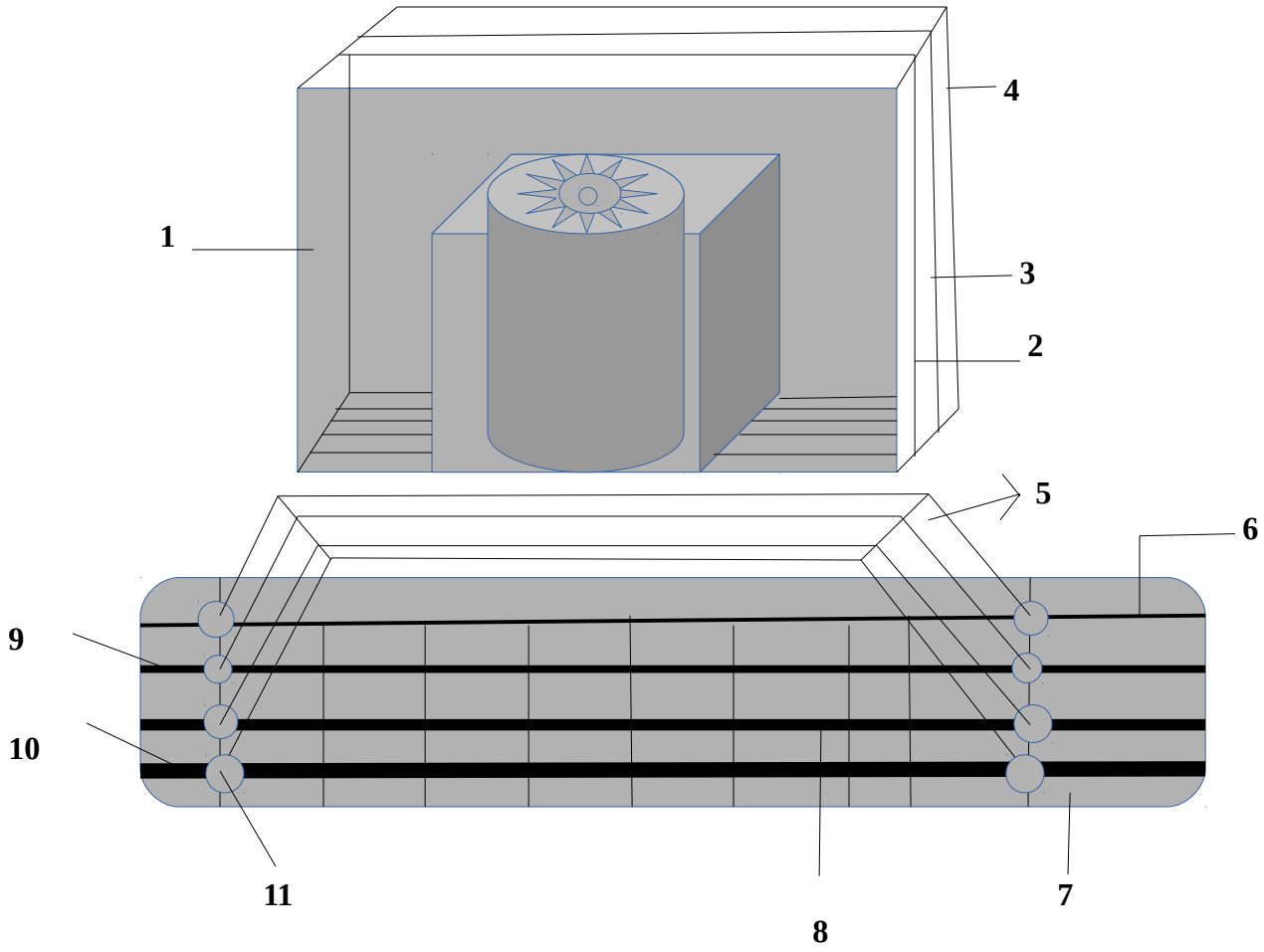
Dual Core Memory Side View

Model Super Sonic 110 Industrial Dual Core CPU Idea 3-A



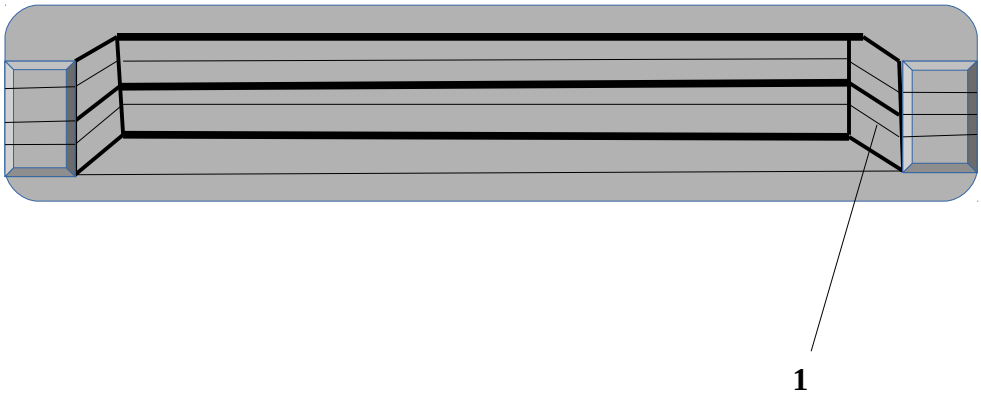
1). Decagon CPU1 layers 1- 10 4096 per layer
2). Decagon CPU 1 Thick Fiber Optic Net
3). Decagon CPU 1 Fitting
4). CPU2
5). CPU 2 Public Area of space 4096 bits for CPU 1
6). CPU 2 Private Area of space 4096 for CPU 1 and CPU2
7). CPU 2 Shared CPU Area of Space 4096 bits for CPU 2
8). CPU 2 Reserved CPU 2 Area of Space 4096 CPU2
9). 4 thin Wires connecting CPU 1 and CPU 2
10). Alternate dual Pipe Wiring path 1 Thick Wiring
11). Alternate dual Pipe Wiring path 2 Thick Wiring
12). CPU 2 Thin Fiber Optic Net
13). CPU2 Buffer area

Model Super Sonic 110 Industrial Video Fan Idea 4- A General View



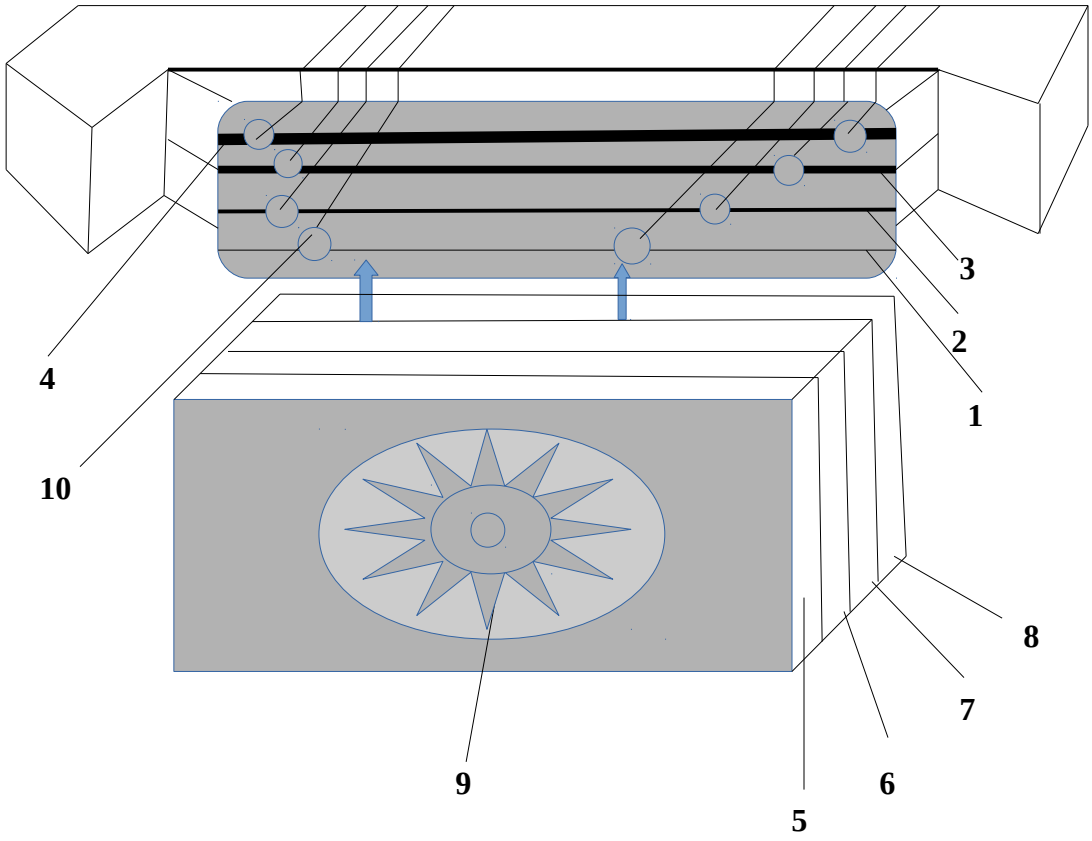
1). Public Video Area Space PKCS12 8192 4096 bit key and 8192 2 sub keys(4096)
2). Private Video Area Space PKCS12 8192 4096 bit key and 8192 2 sub keys(4096)
3). Shared Video Area Space PKCS 12 8192 4096 bit key and 8192 2 sub keys(4096)
4). Reserved Video Area Space PKCS12 8192 4096 bit key and 8192 2 sub keys(4096)
5). Video Data Bride 4 slots
6). Public Data String
7). Titanium video fitting
8). Shared Data String
9). Private Data String
10). Reserved Data String
11). Node Points (End to End point connection)

Model Super Sonic 110 Industrial Patent video slot 5-A General View



1) **Side view of the slot where the Video Card is placed.**

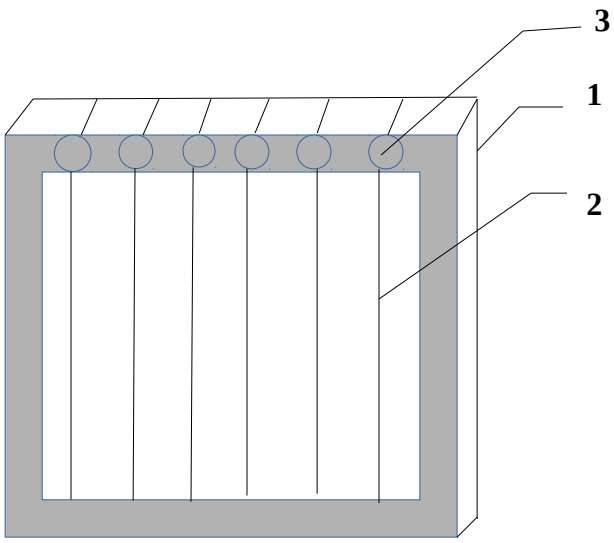
Model Super Sonic 110 Industrial Video slot specs Idea 6-A General View



1	**Public Data String with 8192 pkcs12 4096 key and 4096 sub key**
2	**Private Data String with 8192 pkcs12 4096 key and 4096 sub key**
3	**Shared Data String with 8192 pkcs 12 4096 key and 4096 sub key**
4	**Reserved Data String with 8192 pkcs12 4096 key and 4096 sub key**
5	**Public Video Slot**
6	**Private Video Slot**
7	**Shared Video Slot**
8	**Reserved Video Slot**
9	**Video Fan**
10	**Node Points**

Model Super Sonic 110 Industrial Idea 7-A General View

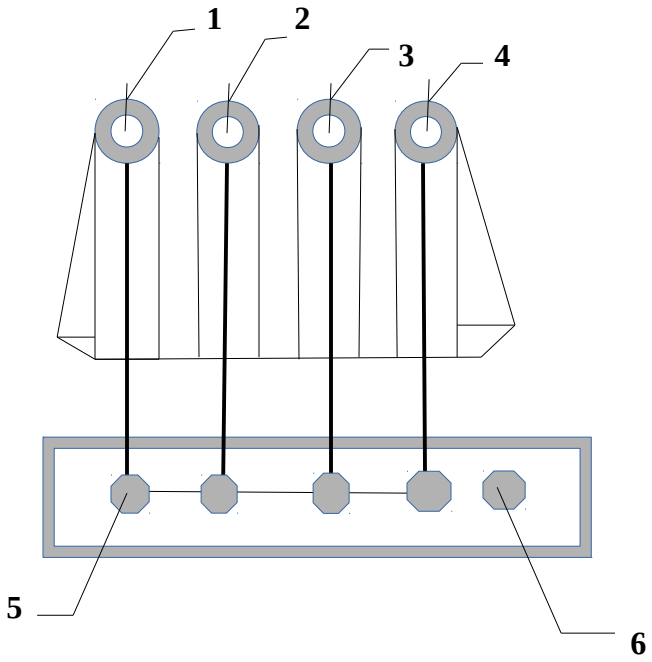
Voltage Regulator 5 wire Check



1). Overall view of chip
2). 6 wires inside chip to check flow of voltage 1024 bits per wire total 6144 bits
3). Node Point check testing wires for on and off conditions

Model Super Sonic 110 Industrial BIOS Idea 8-A General View

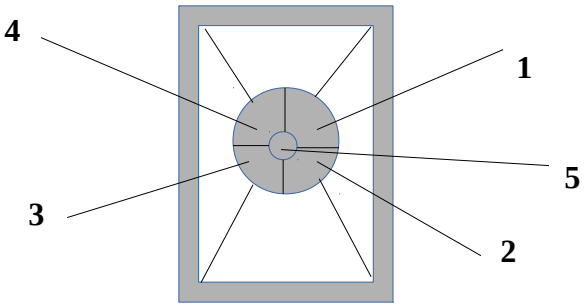
4/5 Pins BIOS



1). Public BIOS Pin
2). Private BIOS Pin
3). Shared BIOS Pin
4). Reserved BIOS Pin
5). BIOS Bins that connect to node Points
6). BIOS Pin Clearing areas of spaces

Model Super Sonic 110 Industrial ROM Chip Idea 9-A General View

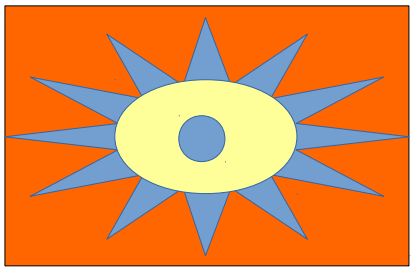
16384 Built in Certificate ROM Chip



1). Public Area of Space
2). Private Area of Space
3). Shared Area of Space
4). Reserved Area of Space
5). Certificate on burned on platter read only

Model Super Sonic 110 Industrial Rom Chip specs Idea 10-A General View

Barrys Scientific Based Products 20480 Bit Hardware Verification Certificate



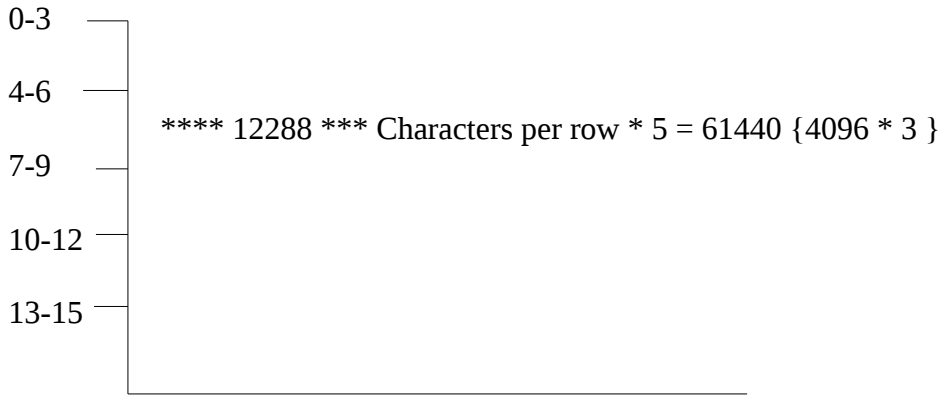
This Certificate is used to check for authenticated Hardware updates it is built into the motherboard via ROM Chip.

1). RSA Sign Only	4096
2). RSA Encrypt 3 sub keys	16384

Chapter 2

Single 61440 Data Block processing

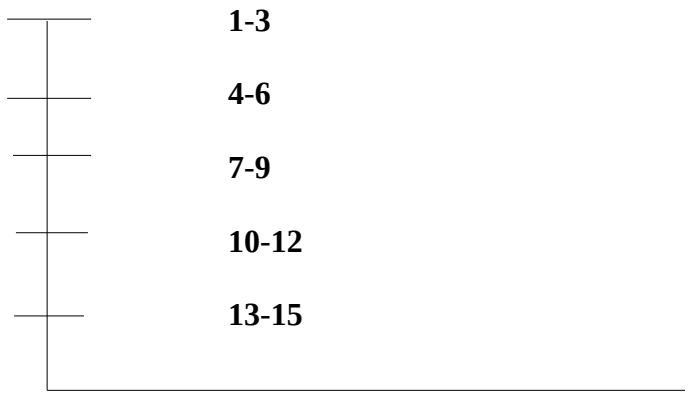
I will begin by defining the block data of 4096 characters total 12288 per packet with the 3072 bit addressing scheme from here I will create a matrix of 15 rows each with 12288 characters matrix. See chart below.
I am going over the method and process defined below.



4096 * 15 rows = 61440 bits

Since I have defined my address scheme as 3072 bits, I divide 61440 by 3072 bits and it comes up with 15 frames. I divide 15 frames by 3 = 5 packets with 3 frames per packet * 4096 byte frames in bursts equals 12288. To secure the data when sending outbound to the Internet or Intranet, I use a frame entanglement swapping frame 0 and 1. This is reassembled at the final destination or hop for old timers also this enforces endpoint to endpoint communication. I create fifteen packets of 4096 byte frames equal to 61440 I can take this further by demanding each packet is authenticated with a 20480 bit certificate held in memory to insure data integrity. If you wish to create an even more secure environment, The user chooses which packets order is to be sent see chart below. I could even swap the last frame's of 14 and 15 with final packet assembly reaching the end point of communication.

Packet #	Frame sequence
1	**1-3**
2	**4-6**
3	**7-9**
4	**10-12**
5	**13-15**



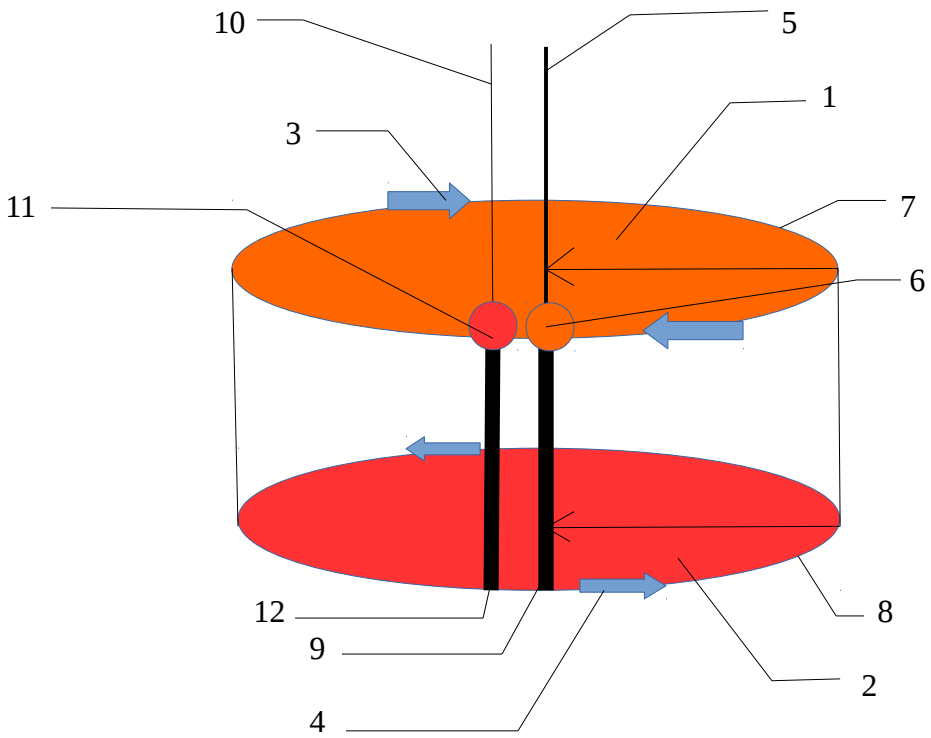
5 packets of 4096 bytes burst with frame sequences of 3. total per packet 3 * 4096= 12288.

1). 61440 / 15 = 4096 per three frames/per packet of 5 bursts

Chapter 3

Cryptographic 800/900 Energy Model Design

Cryptographic 800/900 Energy Model Visual Design



1. Curvature Motion light Energy
2 Curvature Motion heavy energy
3. Clockwise motion
4. Counter Clockwise Energy Regeneration
5. 1st Data String a 1024 bits a
6. Gateway Check node point 1st dimension
7. Orange Elliptic curve 997 Bits
8. Red Elliptic Curve 1229 Bits
9. 2nd Data String a 1536 Bits
10 1st Data String b 2048 Bits 2nd Dimension
11 Gateway Checkpoint 2nd Dimension
12 2nd Data String b 3072 Bits 2nd dimension

Cryptographic 800/900 Energy Model Design Method and Process

I will now present a New Cryptographic Energy Design based on Dynamic Heat and Asymmetrical Energy principles and applications. I will be discussing the method and process of this model

As you can see the energy in chart 1-B curvature is represented by shades of Orange and Red -color spectrum's. The 1st curvature uses 997 bits and the 2nd uses 1229 for a total of 2226 bits. Depending on the number of cycles used examples 13 and 17 I can generate 997 * 13 = 12961 bits + 1229 * 17 = 33854 bits total bits. 33854 < 81920 The system architecture can only support 81920 bits so the number of cycles could support asymmetrical cycles 13 and 17. To complete the processing I must now add the linear strings of the following

1st data string a = 1024
1st data string b = 2048
2nd data string a = 1536
2nd data string b = 3072

data array = 41534 (elliptic) + 1024 + 2048 + 1536 + 3072 (linear) = 7680 this system supports this model because 49214< 81920

The Cryptographic models are based on the Color spectrum's when crossing to dimensional space in relations to linear based strings. The Elliptic colors use more heat and energy as well.

If I set up a series of arrays we could find the total number of bits based on the following example above

1st Curvature = a
2nd Curvature = b
1st data string = c
2nd data string =d
a= 12961
rem 1st curvature 997 *13 cycles

b= 33854
rem 2nd curvature 1229 * 17 cycles
c = 1024
d = 2048
e= 1536
f = 3072

array-1 = {a,b}
rem curvature
array-2 = {c,d,e,f}
rem linear
array-3 = array-1 + array-2
array-3 =41534+7680 = 49214 bits

This system design could support this Cryptographic model because 49214 < 81920 bits

This model uses a combination of both Linear and Curvature motion and Color spectrum Energy equating to a Cryptographic model design as discussed in previous copyrighted models this is being employed and in fact is being improved upon.

I can now subtract 81920 – 49214 and now have =32706 bits to use for my password encryption.

This model uses a combination of both Linear and Curvature motion and Color Spectrum Energy equating to a Cryptographic model design as discussed in previous copyrighted models this is being employed and in fact is being improved upon. I would like to add that because I have 32706 bits I could also create a cryptographic password that insures each IP Packet Integrity and authenticity example:

1). I can use a Data string of 768 bits create parallel strings name it p1+ and p2- The user chooses either p1+ or p2- and than access the curvature space using a prime number of 997 bits with 20 cycles= 19940 bits. The next step is to add the 768 bits = 20708 bits to use for password security. The Equation can be written as follows:

Z {p1+,P2-} = 512 bits Linear

Y = 19940 bits= Curvature

W = Z + Y

B = W/1
B= W/2
B= W/4

I have created three spaces that can be used to break bits into chunks of data this creates a mechanism for multiple paths the final product is below:

B = 20708/1 = 20708
B = 20708/2 = 10354
B= 20708/4 = 5177

To reverse this you simply take the final product * the number being divided example:

5177 *4 = 20708

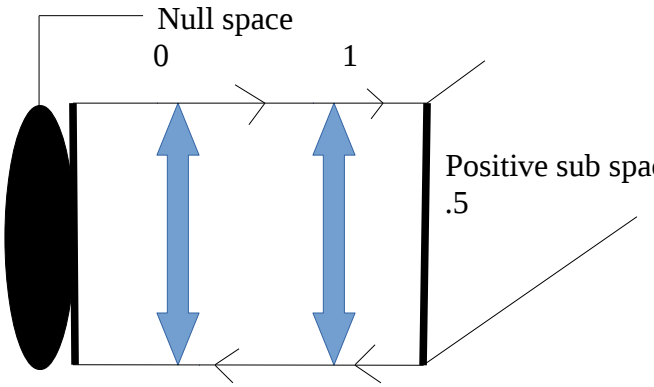
If you will notice, I have 32706 – 20708= 11998 bits left over, This needs to be utilized and how this can be used is by padding the password encryption with the spare bits. This can be achieved by the following:

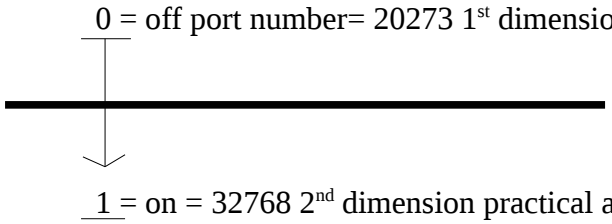
32706 – 20708 = 11998 bits

B =32706/1 =20708 + 11998 Bits

B = 11998/2 = {5999 + 1}1st subscript + {5998+0}2nd subscript total = 11998 . Thus I have created a double subscript for password and padding a IP packet that needs protection. If I want to add extra protection for each subscript simply compress both scripts. If you will notice in the 1st and 2nd subscript, I can create a binary switch "0 = off" and "1=on" to turn password and padding on or off for this particular design for better data protection at users discretion. This can be further expanded to include 4 conditions see visual Picture and table below.

Example Video device





Testing conditions

1) 0 = off 1= on port number 20100
2) 1 = on 0 = off port number 20273
3) .5 = subspace of 1 binary switch off dimensional space is positive port switch redirected to port 32768 with positive area of space
4) -.5= subspace of 0 binary switch is off dimensional space is negative port switch redirected to “null space” void” space.

The purpose of adding two additional testing conditions are the following:

1). Create fractional time space see numbers 3 and 4.

2). Creates a fractional time space where the switch is in the off position but creating positive energy **item number 3** is off but has a fractional time space or 2^{nd} dimensional space of on positive energy.

a). example I have switch off = 0 but really in the on position 1 so 0 | 1| + 2^{nd} dimension positive

3). Creates a fractional Space where the switch is in the off position but creates negative energy see **item number 4** is in the binary switch position of off but has a fractional time space or 2^{nd} dimensional space of negative energy.

b). example I have a switch off = 0 but really in the on position 1 so 0| 1| - 2^{nd} dimension space

This creates a way to test for fractional time space also in consideration a practical application is to turn the switch off on the port number and have it redirected to a port switch in the on position. The negative space is given a “null space” . Please notice the kinetic energy in the graph 2^{nd} dimensional spacing linear and curvature. This opens the door utilizing authenticating port numbers with linear and circular certificates for validation purposes.

The next item to be discussed is the password process please see below:

{5999+1 = √6000 = 77.4596669241st subscript the 2^{nd} subscript 5998+0 = √5998=77.446755904 I have compressed both of these because of the principles of asymmetry not balanced form of energy and discreet energy numbers with the deciding factor belonging to the binary switch off and on hidden variable principle, theory, and application.

The equation could be written as such ($\sqrt{\text{a and or b}}$) = d

I will now write my final thoughts on this Projects

Final Thoughts

Chapter 4

I have improved upon my CPU Model by adding layered models for CPU 1 and 2 that are asymmetrical in nature one supports 10 layers the other supports 5 layers for a total of 61440 bits the CPU can support ;however, the memory supports 81920 bits with a buffer chip to que the overflow from the Memory to the CPU's. This model is updated from three to four thin wires on the CPU.

This project involved making improvements on prior existing designs along with modifications. I also created a password algorithm for this project along with padding also created subscripts used for padding the address spaces creating a extra layer of IP packet protection along with password protection.

The Video card has been updated to provide some level of privacy and security using PKCS12 8192 bits per area 4096 bit keys and two 4096 bit sub keys total 4 areas of space * 12288 bits = 49152 bits. This can be done creating 4096 PKCS12 and two sub keys total 8192 bits.

The Cryptographic model with dynamic linear strings and dual curvature blocks also I have created a built in 20480 ROM certificate 1 RSA sign and 3 sub keys demonstrating principles of Dynamic Energy being deployed also introduced added is a way to use port redirects with Certificate Validation using both Linear and Elliptic Kinetic Energy creating fractional space time in a practical application sense.

I have reached the outer limits of this cryptographic model and this will be revamped to reflect the upgraded design for the 4^{th} generation.

If you wish to view more work, Please visit my website below

www.barrysscientificbasedproducts.info

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2/13/2019

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