# Barrys SS-89-A Motherboard Design

**by**

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## Introduction

I would like to take the time in Thanking each and everyone of you for reading this Science and technology based work. I have made improvements on the SS-87 Motherboard Design please view the following below:

1). The Visual **Model Super Sonic 89 Motherboard 1-A General View** overall view of the product and demonstrates a Industrial Design because of it's unique characteristics. The detailed features that are within the Design accompanies in views 2-a through 9-A with detailed specs. The features of this design comes with a CPU that can make path choices either using 3 thin wires or 1 thick wire to access each CPU based on Intelligent Design paths.

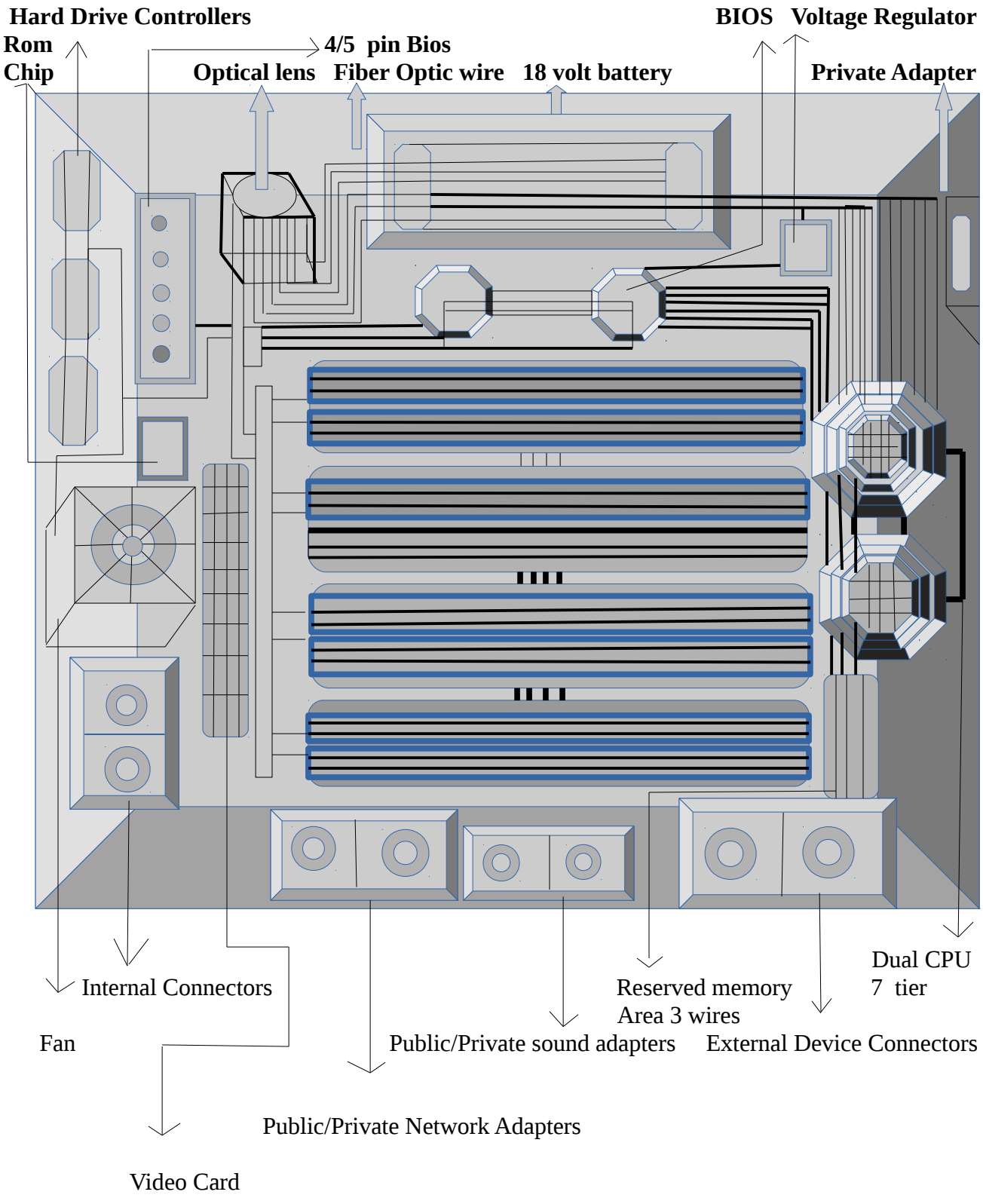
2). **Patent Ideal 2 Method and Single 24576 Data Block processing. T**his is discussed as a method and process of Internal Packet exchanges within the Motherboard Design itself and is upgraded as well.

3). **Patent Idea New Cryptographic Energy Model Design.** This is shown as an Industrial Design along with the method and process. This comes with parallel 512 bit data strings and a password encryption and padding Mathematical equation with process and method.

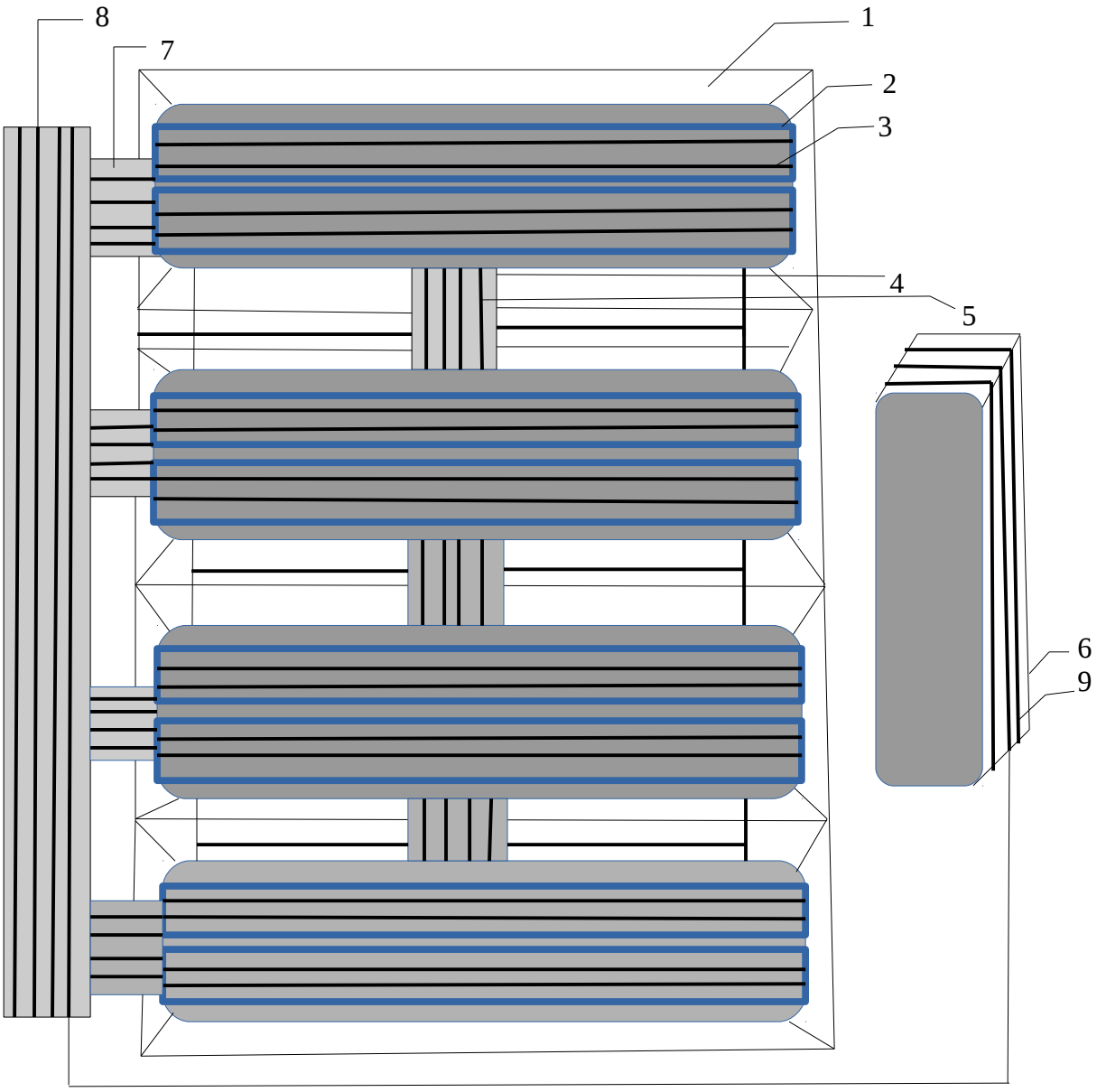
This is a 3rd generation motherboard Design. Once again thank you for reading this work !

## Table of Contents

**Model Super Sonic 89-A Motherboard- Design 1-A General View**

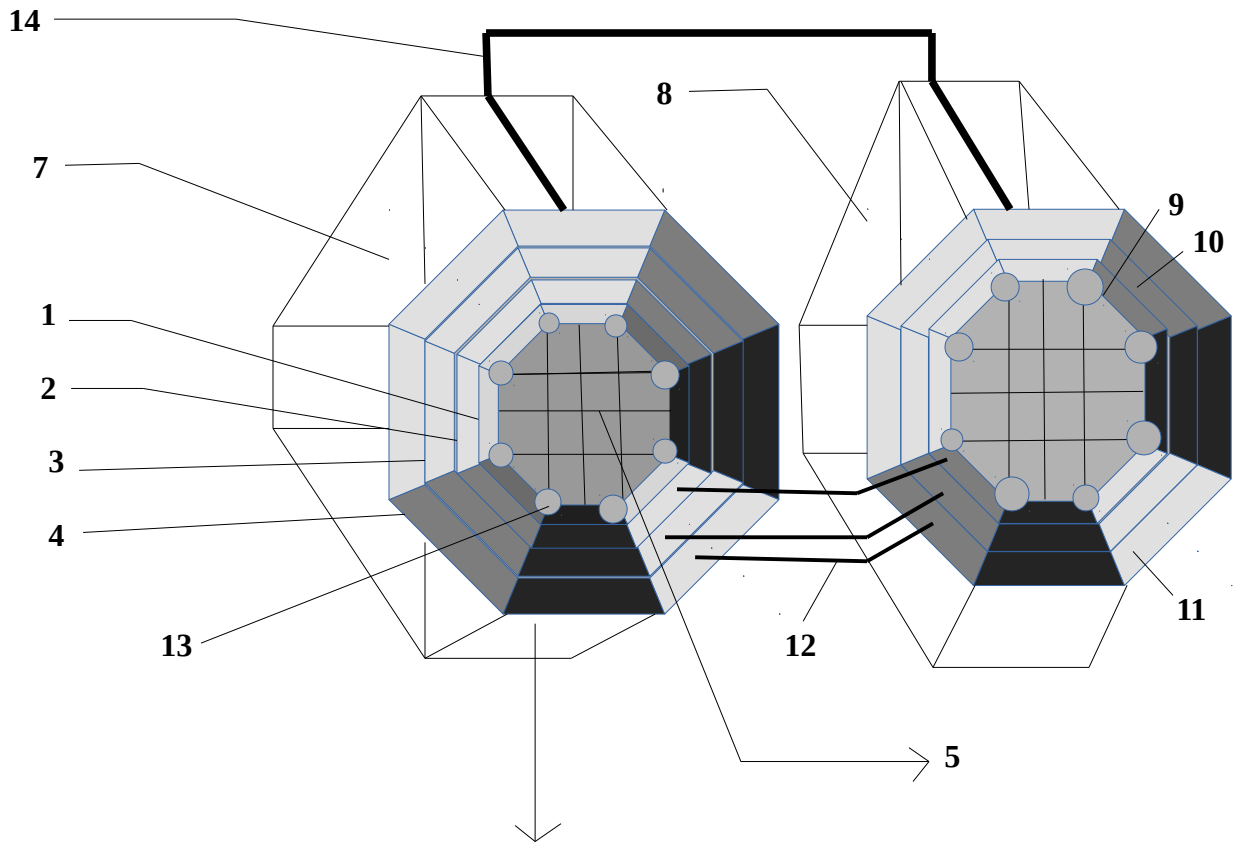


**Model Super Sonic 89-A Motherboard memory chip Idea 2-A**



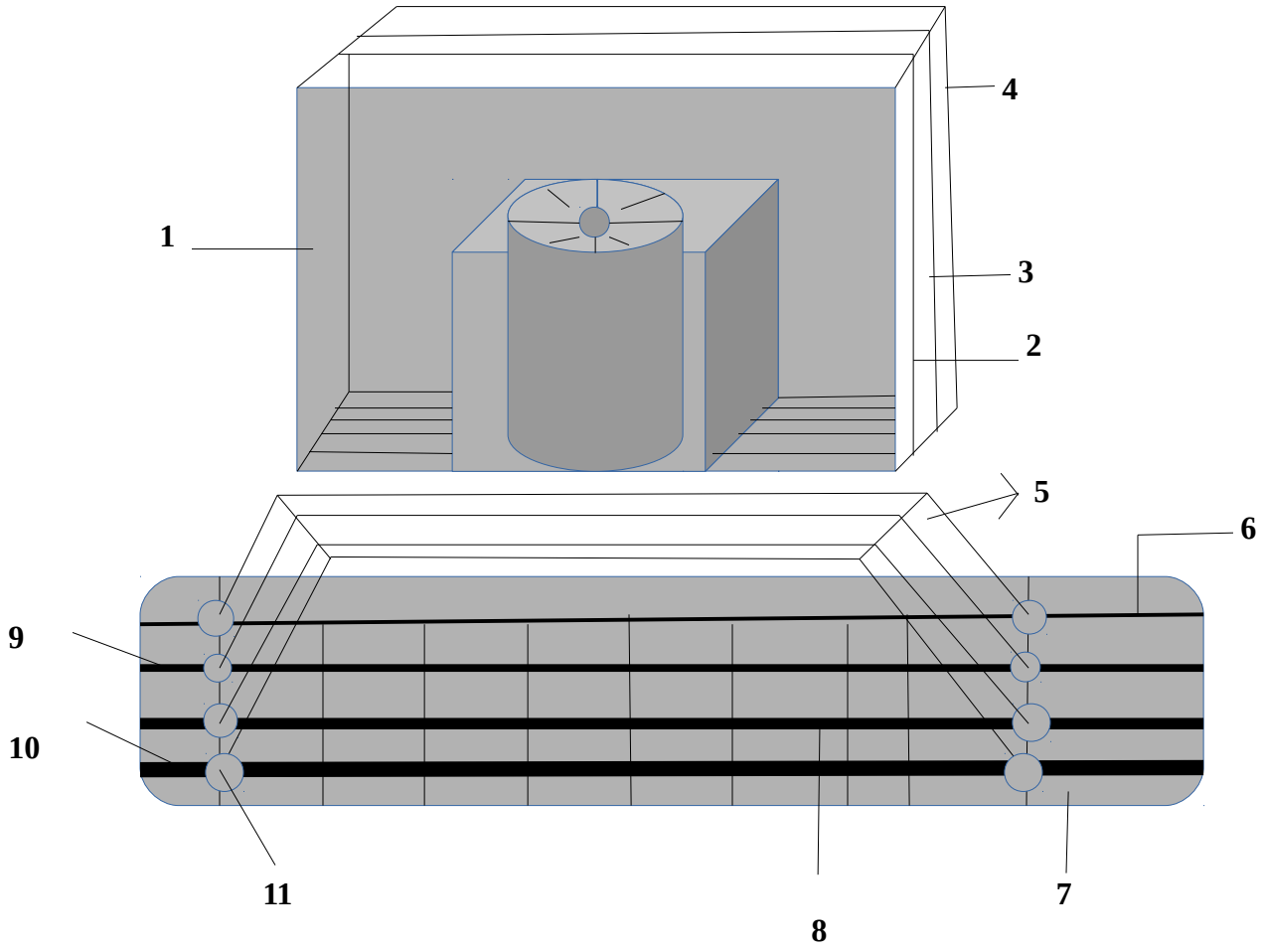

1). Fitting to hold Memory Chips
2). Banks 2 banks per memory chip 512 per bank total 1024 bit addressing scheme
3). Data Strings 2 strings per Bank 256 bits per string total 4 strings per chip 1024 bit addressing
4). Area Memory Bridge (Bytes to Frames switches)
5). 4 data strings per bridge 256 bits per wire total 1024 bits
6). Reserved Memory area (Buffer) 3072 bits
7). Fiber Optic tube address encasement
8). Address Bridge 4 wires 256 bits per wire to process Fiber Optic
9). three Data wires for holding in reserved space 1024 per wire

**Model Super Sonic 89-A Industrial CPU Idea 3-A**



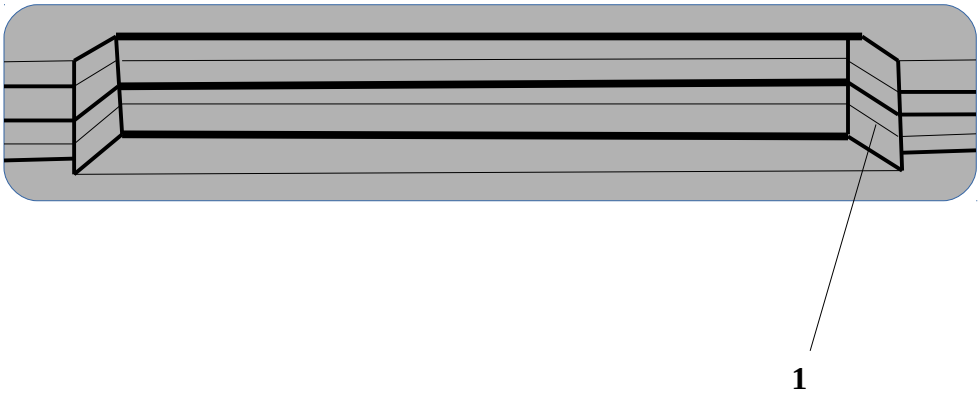

**1). Public CPU 1 Area of Space 4096 Bits CPU 1**
**2). Private CPU 1 Area of Space 4096 Bits CPU1**
**3). Shared CPU 1 Area of Space 4096 CPU1**
**4). Reserved CPU 1 Area of Space 4096 Bits CPU1**
**5). Fiber Optic Net**
**6). CPU Fitting**
**7). CPU 1**
**8). CPU2**
**9). CPU 2 Reserved Area of space 4096 bits for CPU 1**
**10). CPU 2 Shared Area of space 2048 for CPU 1 and CPU2**
**11). CPU 2 Reserved CPU Area of Space 2048 bits for CPU 2**
**12). 3 thin Wires connecting CPU 1 and CPU 2**
**13). Gateway Node Points**
**14). Alternate Wiring path 1 Thick wiring**

**Model Super Sonic 89-A Industrial Fan Idea 4- A General View**



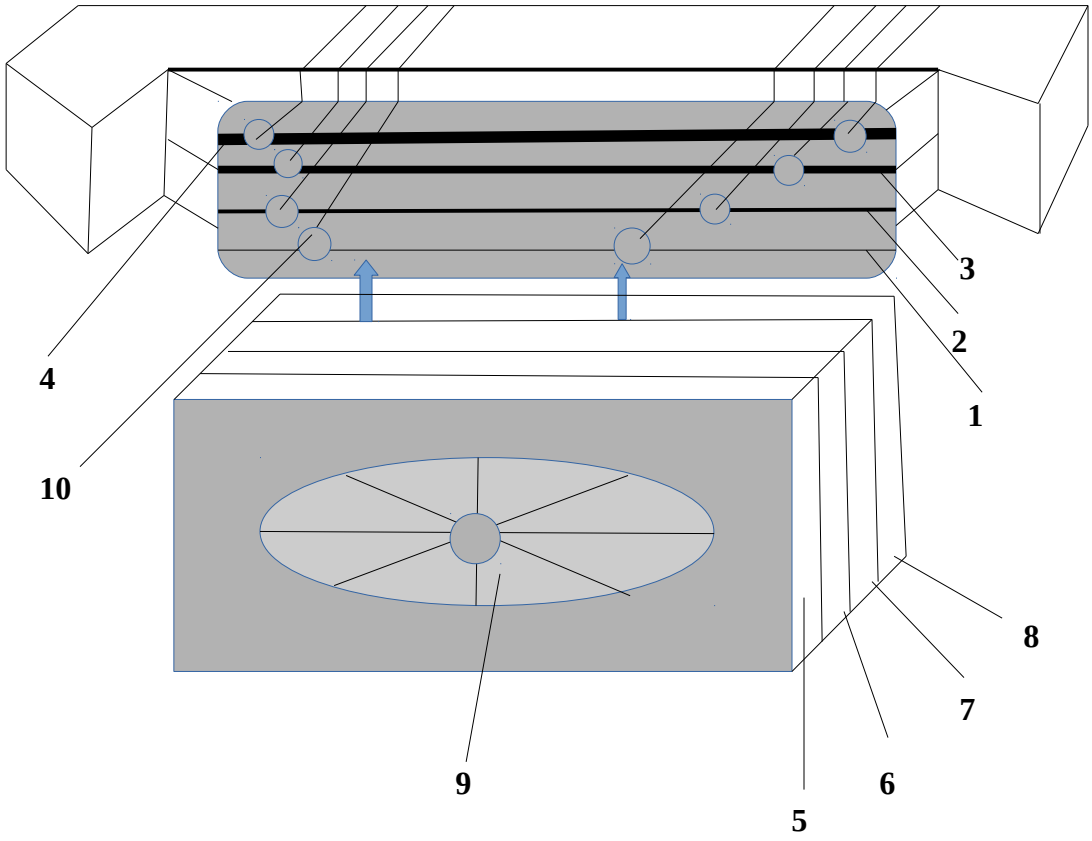

1). **Public Video Area Space**
2). **Private Video Area Space**
3). **Shared Video Area Space**
4). **Reserved Video Area Space**
5). **Video Data Bride 4 slots**
6). **Public Data String**
7). **Titanium video fitting**
8). **Shared Data String**
9). **Private Data String**
10). **Reserved Data String**
11). **Node Points (End to End point connection)**

**Model Super Sonic 89-A Industrial Patent video slot  5-A General View**




1) **Side view of the slot where the Video Card is placed.**

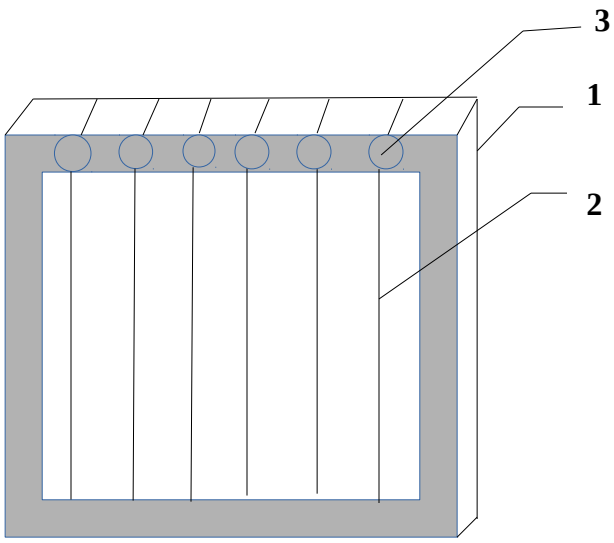
**Model Super Sonic 89-A Industrial Video slot specs Idea 6-A General View**




| | |
|---|---|
| 1 | Public Data String 256 bits |
| 2 | Private Data String256 bits |
| 3 | Shared Data String 256 bits |
| 4 | Reserved Data String 256 Bits |
| 5 | Public Video Slot |
| 6 | Private Video Slot |
| 7 | Shared Video Slot |
| 8 | Reserved Video Slot |
| 9 | Video Fan |
| 10 | Node Points |

**Model Super Sonic 89-A Industrial Idea 7-A General View**

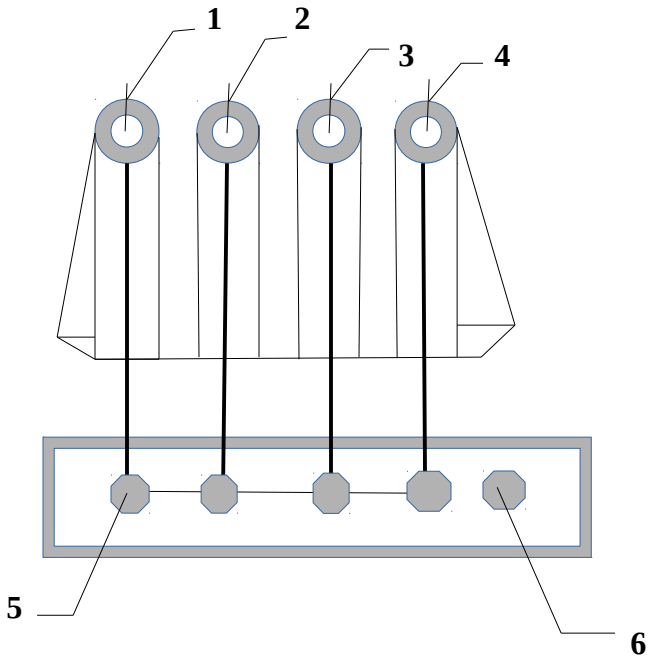
**Voltage Regulator 5 wire Check**




**1). Overall view of chip**
**2). 6 wires inside chip to check flow of voltage 1024 bits per wire total 6144 bits**
**3). Node Point check testing wires for on and off conditions**

**Model Super Sonic 89-A Industrial Bios Idea 8-A General View**

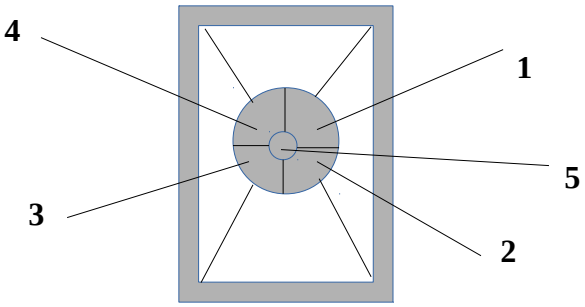
**4/5 Pins Bios**




**1). Public Bios Pin**
**2). Private Bios Pin**
**3). Shared Bios Pin**
**4). Reserved Bios Pin**
**5). Bios Bins that connect to node Points**
**6). Bios Pin Clearing areas of spaces**

**Model Super Sonic 89 Industrial ROM Chip Idea 9-A General View**

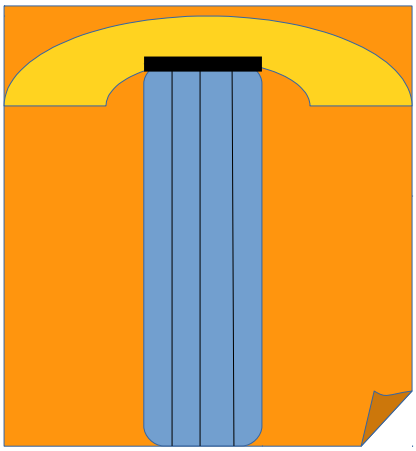
**15360 Built in Certificate ROM Chip**




**1). Public Area of Space**
**2). Private Area of Space**
**3). Shared Area of Space**
**4). Reserved Area of Space**
**5). Certificate on burned on platter read only**

**Model Super Sonic 89 Industrial Rom Chip specs Idea 10-A General View**

**Barrys Scientific Based Products 15360 Bit Hardware Verification Certificate**



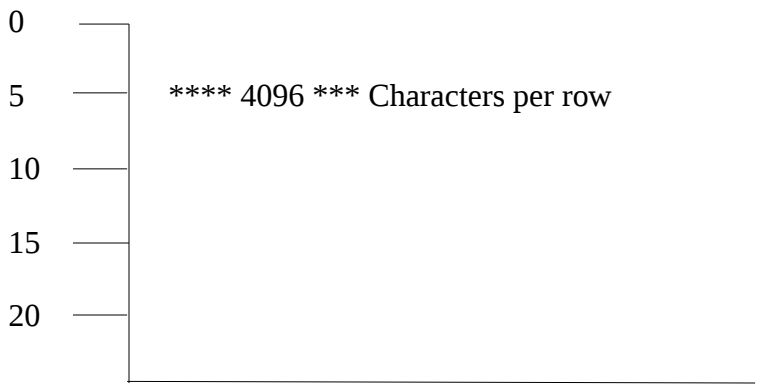
This Certificate is used to check for authenticated Hardware updates it is built into the motherboard via ROM Chip.

| | |
|---|---|
| 1). RSA Sign Only | 3072 |
| 2). RSA Encrypt 3 subkeys | 12288 |

# Chapter 2

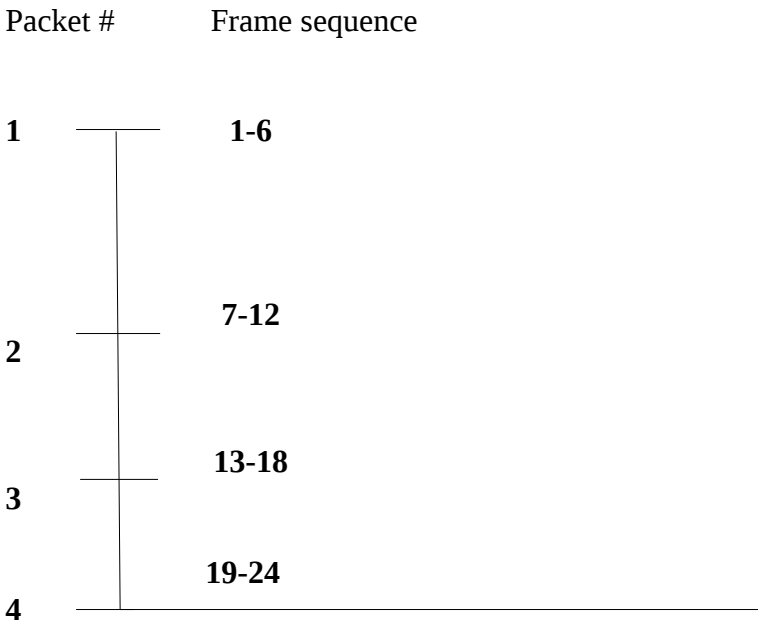
## Single 24576 Data Block processing

I will begin by defining the block data of 4096 characters with the 1024 bit addressing scheme from here I will create a matrix of 6 rows each with 4096 characters matrix. See chart below. I am going over the method and process defined below.




4096 * 6 rows = 24576 bits

Since I have defined my address scheme as 1024 bits. I divide 24576 by 1024 bits and it comes up with 24 frames. I divide 24 frames by 4 = 6 frames * 4096 byte frames in bursts equals 24576. To secure the data when sending outbound to the Internet or Intranet, I use a frame entanglement swapping frame 1 and 2. This is reassembled at the final destination or hop for old timers also this enforces endpoint to endpoint communication. I create six packets of 4096 byte frames equal to 24576 I can take this further by demanding each packet is authenticated with a 12288 bit certificate held in memory to insure data integrity. If you wish to create an even more secure environment, The user chooses which packets order is to be sent see chart below. I could even swap the last frame's of 23 and 24 with final packet assembly reaching the end point of communication.

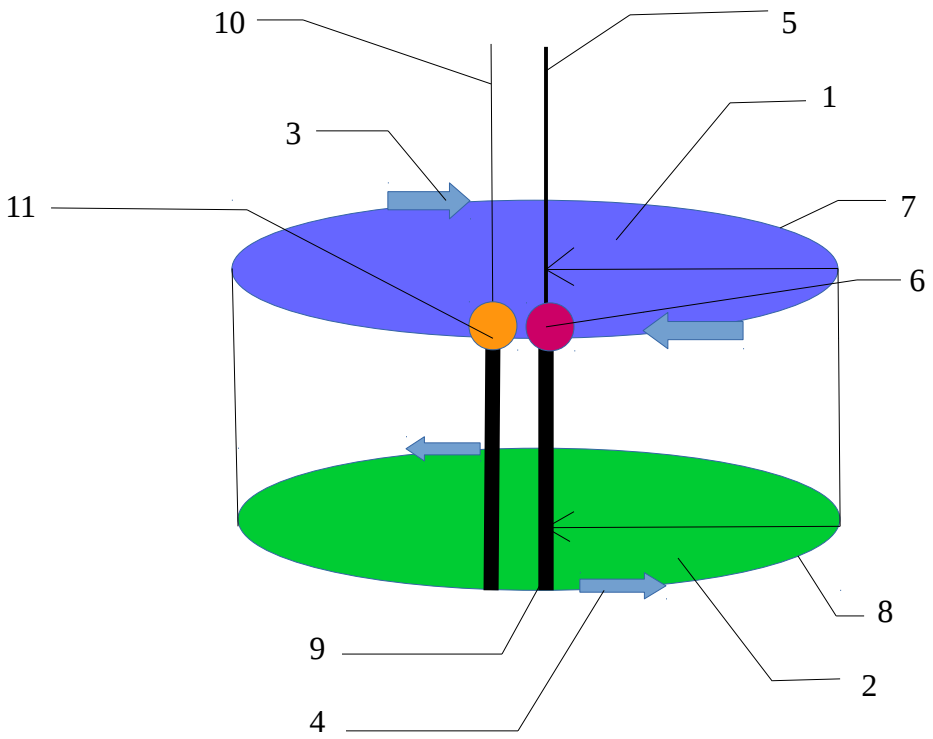



**4 packets of 4096 bytes burst with frame sequences of 6.**

# Chapter 3

# New Cryptographic Energy Model Design

**Cryptographic Energy Model Visual Design**




1. Curvature Motion light Energy
2 Curvature Motion heavy energy
3. Clockwise motion
4. Counter Clockwise Energy Regeneration
5. 1st Data String 512 bits
6. Gateway Check node point 1st dimension
7. Blue Elliptic curve 827 Bits
8. Green Elliptic Curve 839 Bits
9. 2nd Data String 768 Bits
10 2nd Data String 512 Bits 2nd Dimension
11 Gateway Checkpoint 2nd Dimension

**Cryptographic Energy Model Design Method and Process**

I will now present a New Cryptographic Energy Design based on Dynamic Heat and Asymmetrical Energy principles and applications. I will be discussing the method and process of this model

As you can see the energy in chart 1-B curvature is represented by shades of blue and green -color spectrum's. The 1st curvature uses 827 bits and the 2nd uses 839 for a total of 1666 bits. Depending on the number of cycles used examples 9 and 11 I can generate 827 * 9 = 7443 bits + 839 * 11 = 9229 bits total 16672 bits. 16672 < 24576 The system architecture can only support 24576 bits so the number of cycles could support asymmetrical cycles 9 and 11. To complete the processing I must now add the linear strings of 512 + 768 = 1280 so 16672 + 1280 =17952 this system supports this model because 17952 < 24576

The Data Strings has the 1st linear string at 512 Bits and the 2nd uses 768. The total is 1280 bits

If I set up a series of arrays we could find the total number of bits based on the following example above

1st Curvature = a
2nd Curvature = b
1st data string = c
2nd data string =d
a= 7443
rem 1st curvature 827 *9 cycles

b= 9229
rem 2nd curvature * 9 cycles
c = 512
d = 768

array-1 = {a,b}
array-2 = {c,d}
array-3 = array-1 + array-2
array-3 =17952+1280 = 19232 bits

This system design could support this Cryptographic model because 19232 < 24576 bits

This model uses a combination of both Linear and Curvature motion and Energy equating to a Cryptographic model design as discussed in previous copyrighted models this is being employed and in fact is being improved upon.

I can now subtract 24576 – 19232 and now have =5344 bits to use for my password encryption.

This model uses a combination of both Linear and Curvature motion and Energy equating to a Cryptographic model design as discussed in previous copyrighted models this is being employed and in fact is being improved upon. I would like to add that because I have 5344 bits I could also create a cryptographic password that insures IP Packet Integrity and authenticity example:

1). I can use a Data string of 512 bits create parallel strings name it p1+ and p2- The user chooses either p1+ or p2- and than access the curvature space using a prime number of 827 bits with 5 cycles= 4135 bits. The next step is to add the 512 bits = 4647 bits to use for password security. The Equation can be written as follows:

Z {p1+,P2-} = 512 bits Linear

Y = 4135 bits= Curvature

W = Z + Y

B = W/1
B=  W/3

I have created two spaces that can be used to break 4647 bits into chunks of data this creates a mechanism for multiple paths the final product is below:

B = 4647/1 = 4647
B = 4647/3 = 1549

To reverse this you simply take the final product * the number being divided example:

1549 * 3 = 4647

If you will notice, I have 697 bits left over, This needs to be utilized and how this can be used is by padding the password encryption with the spare bits. This can be achieved by the following:

5344 – 4647 = 697 bits

B =4647/1 =4647 + 697 Bits

B = 4647/3 = {1549 + 232}1st subscript + {1549+232}2nd subscript + {1549+233}=5344 3rd subscript. Thus I have created a 1549/232 triple subscript for password and padding a IP packet that needs protection.

I will now write my final thoughts on this Projects

# Final Thoughts

## Chapter 4

I have improved upon my CPU Model by using Alternate Path usage. The CPU can have the ability to make choices that is best suited for processing example The CPU can take the 1st choice of accessing the three thin wires or the other choice using the 1 thick wire depending on the metrics of throughput usages.

This project involved making improvements on prior existing designs along with modifications. I also created a password algorithm for this project along with padding also created subscripts used for padding the address spaces creating a extra layer of IP packet protection along with password protection.

I also updated the Cryptographic model with dual 512 bit linear strings also I have created a built in 15360 ROM certificate 1 RSA sign and 3 subkeys demonstrating principles of Dynamic Energy being deployed.

If you wish to view more work, Please visit my website below

www.barrysscientificbasedproducts.info

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10/01/2018

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