Barrys SS-87 ver 1.1 Motherboard Design 3rd Generation

by

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Introduction

I would like to to thank each and everyone of you for taking the time in reading this work. I originally submitted the SS-87 as a Provisional Patent with the USPTO but I was unable to work things out so I have decided to submit it as a copyright with improvements in the CPU including extra wiring thick for alternative path usage one thick wire verse 3 thin wires, 12288 built in ROM Certificate Assymterical, and a encrypted password model, application, and Mathematical Equation with reverse engineering using multiple paths.

1). The Visual design **Model Super Sonic 87 Motherboard** with detail specification on each component along with visual views

2). **Method and Single 20480 Data Block processing. T**his is discussed as a method and process of Internal Packet exchanges within the Motherboard Design itself

3). **New Cryptographic Energy Model Design.** There are three parts to this the 1st is the visual display of the model linear and curvature the process of using a block of data and finally a password encryption model that also employs multiple paths, motion and reverse engineering processes along with a mathematical equation working within the 20480 Data block. This chapter also emphasizes usage of prime numbers.

The Model Super Sonic 87 is a third generation of Motherboard Designs.

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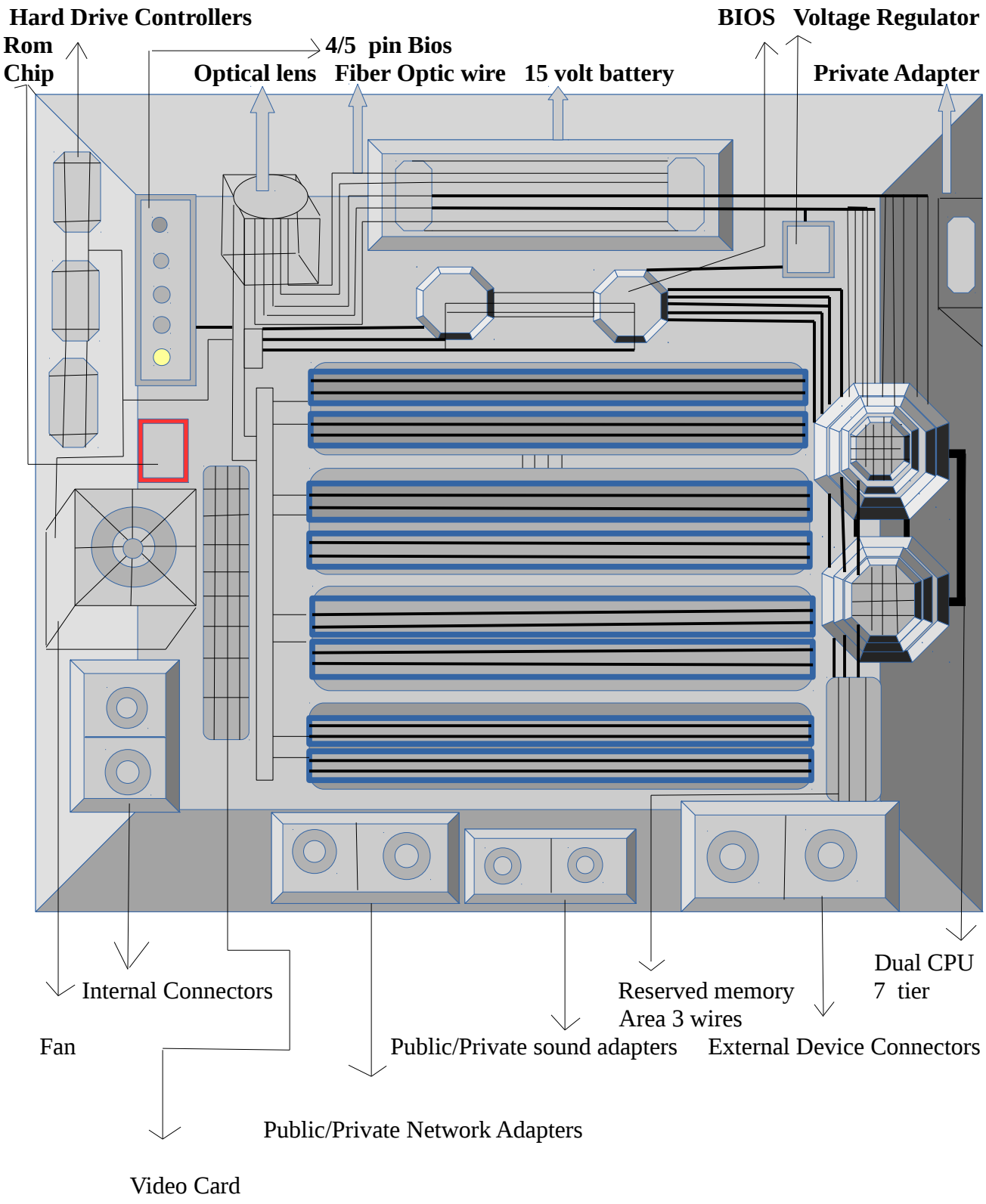
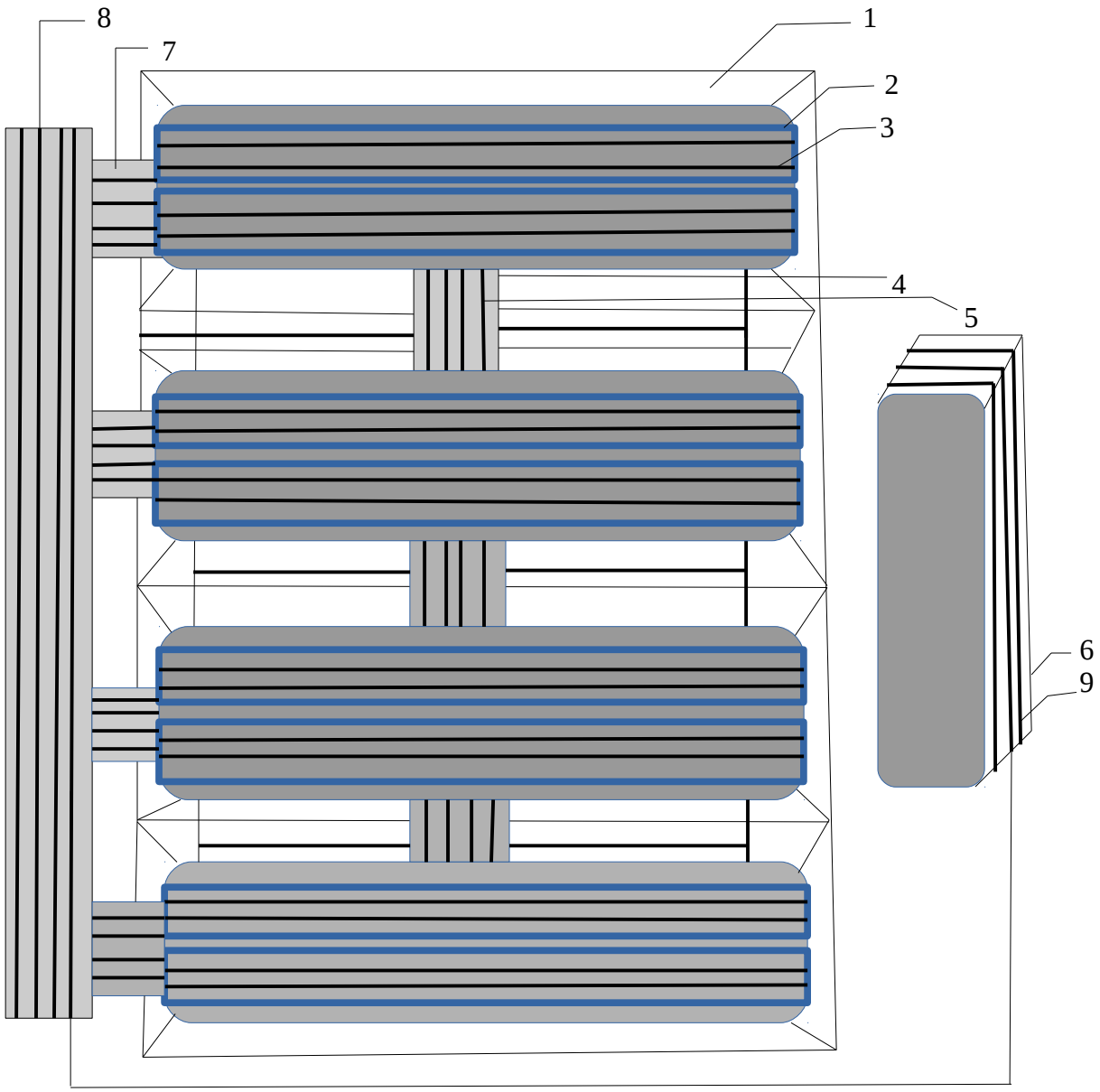
Model Super Sonic 87 Motherboard- Design Visual Display

Chapter 1

Model Super Sonic 87 Motherboard- Design General View 1-A

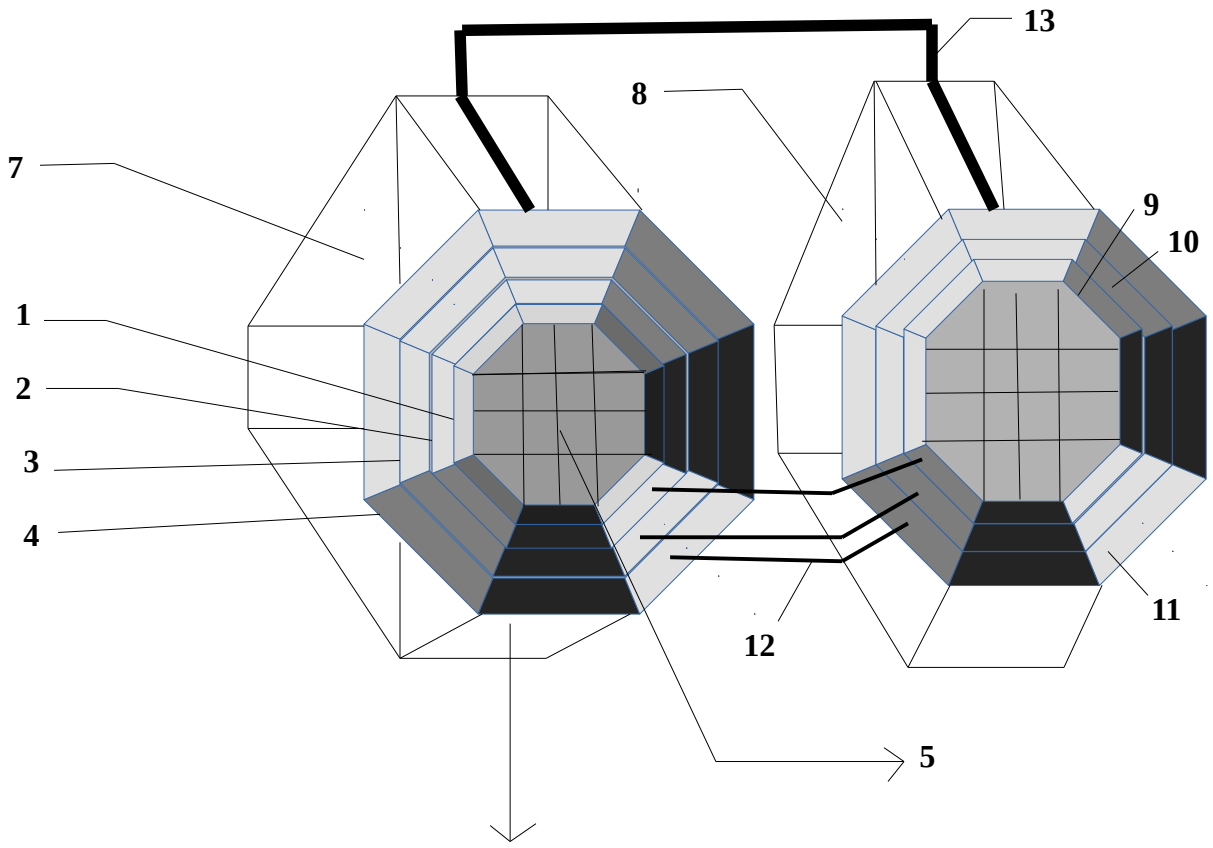


Model Super Sonic 87 Memory Chip view 2-A



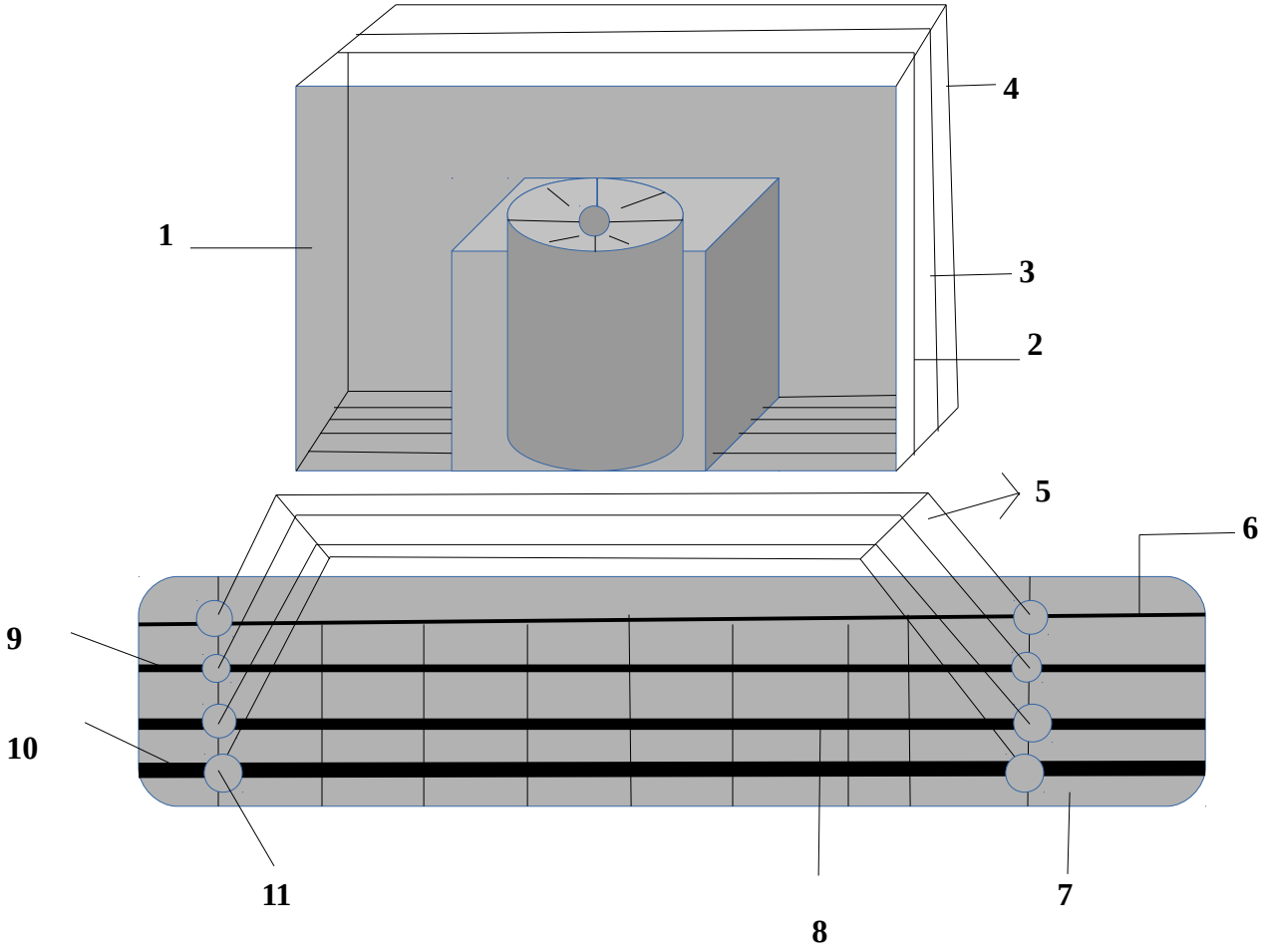
1). Fitting to hold Memory Chips
2). Banks 2 banks per memory chip 512 per bank total 1024 bit addressing scheme
3). Data Strings 2 strings per Bank 256 bits per string total 4 strings per chip 1024 bit addressing
4). Area Memory Bridge (Bytes to Frames switches)
5). 4 data strings per bridge 256 bits per wire total 1024 bits
6). Reserved Memory area (Buffer) 3072 bits
7). Fiber Optic tube address encasement
8). Address Bridge 4 wires 256 bits per wire to process Fiber Optic
9). three Data wires for holding in reserved space 1024 per wire

Model Super Sonic 87 CPU View 3-A



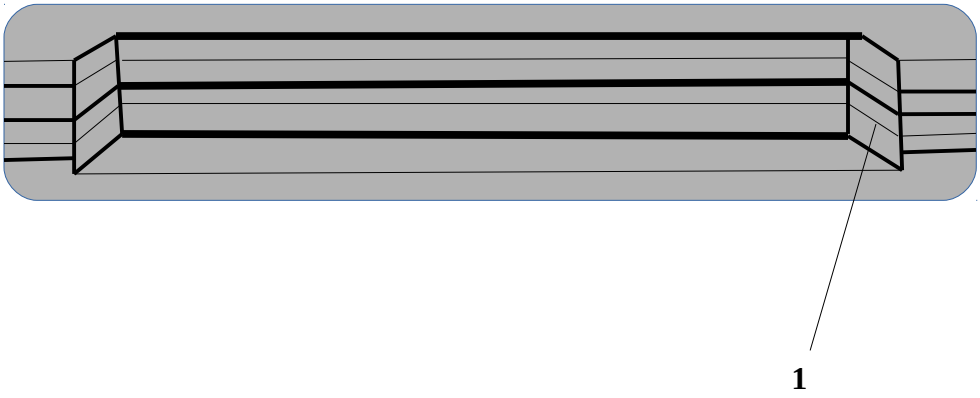
1). Public CPU 1 Area of Space 4096 Bits CPU 1
2). Private CPU 1 Area of Space 4096 Bits CPU1
3). Shared CPU 1 Area of Space 4096 CPU1
4). Reserved CPU 1 Area of Space 4096 Bits CPU1
5). Fiber Optic Net
6). CPU Fitting
7). CPU 1
8). CPU2
9). CPU 2 Reserved Area of space 1024 bits for CPU 1
10). CPU 2 Shared Area of space 2048 for CPU 1 and CPU2
11). CPU 2 Reserved CPU Area of Space 1024 bits for CPU 2
12). 3 Wires connecting CPU 1 and CPU 2
13 1 = 3 wires thick connecting CPU1 and CPU 2 – Alternative path usage

Model Super Sonic 87 Video card General View 4-A



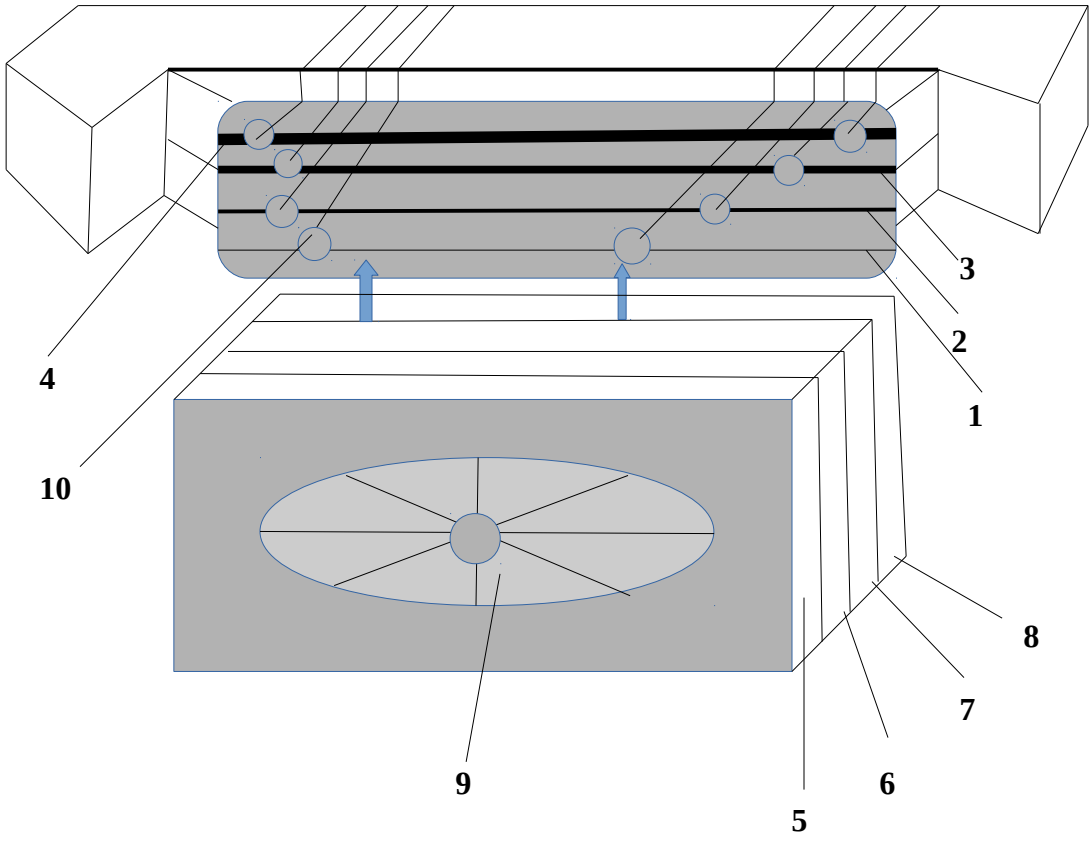
1). **Public Video Area Space**
2). **Private Video Area Space**
3). **Shared Video Area Space**
4). **Reserved Video Area Space**
5). **Video Data Bride 4 slots**
6). **Public Data String**
7). **Titanium video fitting**
8). **Shared Data String**
9). **Private Data String**
10). **Reserved Data String**
11). **Node Points (End to End point connection)**

Model Super Sonic 87 Memory slot card view 5-A



1) **Side view of the slot where the Video Card is placed.**

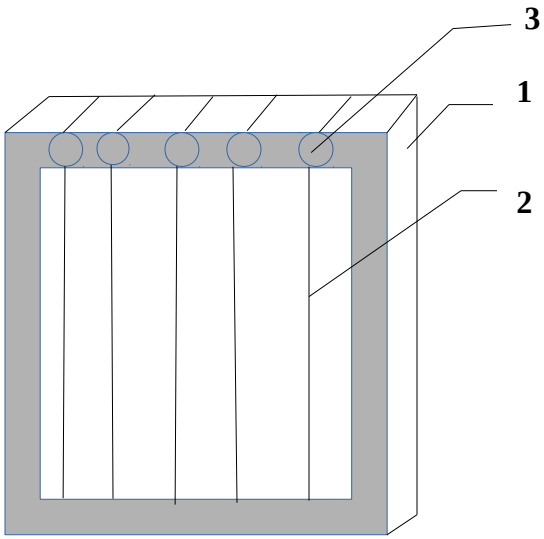
Model Super Sonic 87 Video Card side View 6-A



1	**Public Data String 256 bits**
2	**Private Data String256 bits**
3	**Shared Data String 256 bits**
4	**Reserved Data String 256 Bits**
5	**Public Video Slot**
6	**Private Video Slot**
7	**Shared Video Slot**
8	**Reserved Video Slot**
9	**Video Fan**
10	**Node Points**

Model Super Sonic 87 Voltage Regulator view 7-A

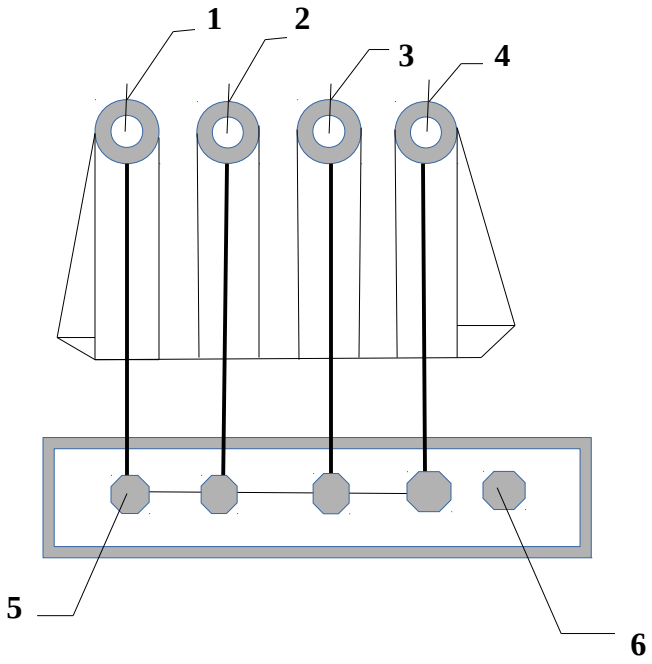
Voltage Regulator 5 wire Check



1). Overall view of chip
2). 5 wires inside chip to check flow of voltage 1024 bits per wire total 5120 bits
3). Node Point check testing wires for on and off conditions

Model Super Sonic 87 Bios chip General View 8-A

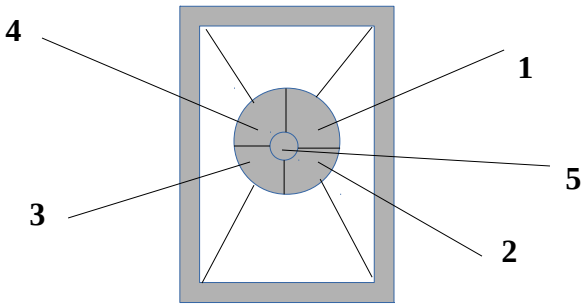
4/5 Pins Bios



1). Public Bios Pin
2). Private Bios Pin
3). Shared Bios Pin
4). Reserved Bios Pin
5). Bios Bins that connect to node Points
6). Bios Pin Clearing areas of spaces

Model Super Sonic 87 Rom Chip General view 9-A

12288 Built in Certificate ROM Chip



1). Public Area of Space
2). Private Area of Space
3). Shared Area of Space
4). Reserved Area of Space
5). Certificate on burned on platter read only

Model Super Sonic 87 Built in Certificate general view10-A

Barrys Scientific Based Products 12288 Bit Hardware Verification Certificate

This Certificate is used to check for authenticated Hardware updates it is built into the motherboard via ROM Chip.

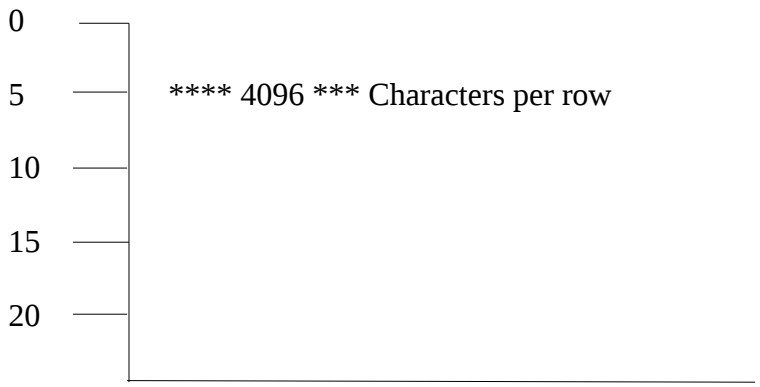
1). RSA Sign Only 4096
2). RSA Encrypt 2 subkeys 8192

The certificate is asymmetrical because the sign does not equal the sub keys and uses a total of 12288 bits

Method and or Process Single 20480 Data Block processing

Chapter 2

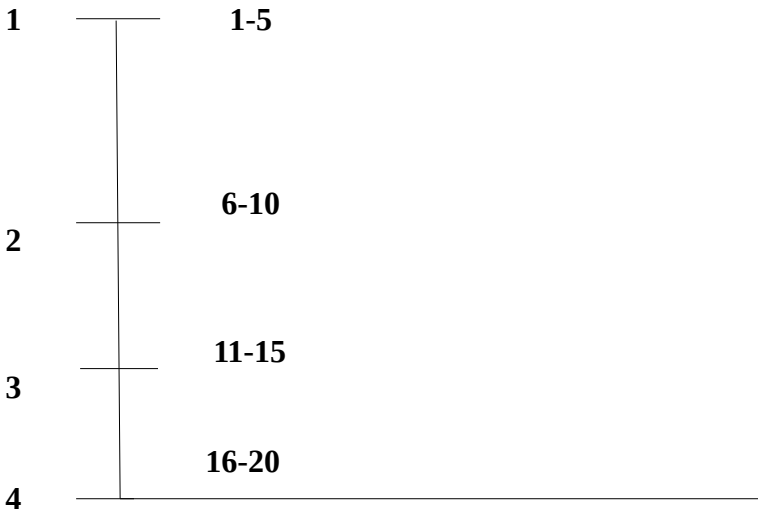
I will begin by defining the block data of 4096 characters with the 1024 bit addressing scheme from here I will create a matrix of 5 rows each with 4096 characters matrix. See chart below. I am going over the method and process defined below.



4096 * 5 rows = 20480 bits

Since I have defined my address scheme as 1024 bits. I divide 20480 by 1024 bits and it comes up with 20 frames. I divide 20 frames by 4 5 frames * 4096 byte frames in bursts equals 20480. To secure the data when sending outbound to the Internet or Intranet, I use a frame entanglement swapping frame 1 and 2. This is reassembled at the final destination or hop for old timers also this enforces endpoint to endpoint communication. I create five packets of 4096 byte frames equal to 20480 I can take this further by demanding each packet is authenticated with a 12288 bit certificate held in memory to insure data integrity. If you wish to create an even more secure environment, The user chooses which packets order is to be sent see chart below. I could even swap the last frame’s of 19 and 20 with final packet assembly reaching the end point of communication.

Packet # Frame sequence

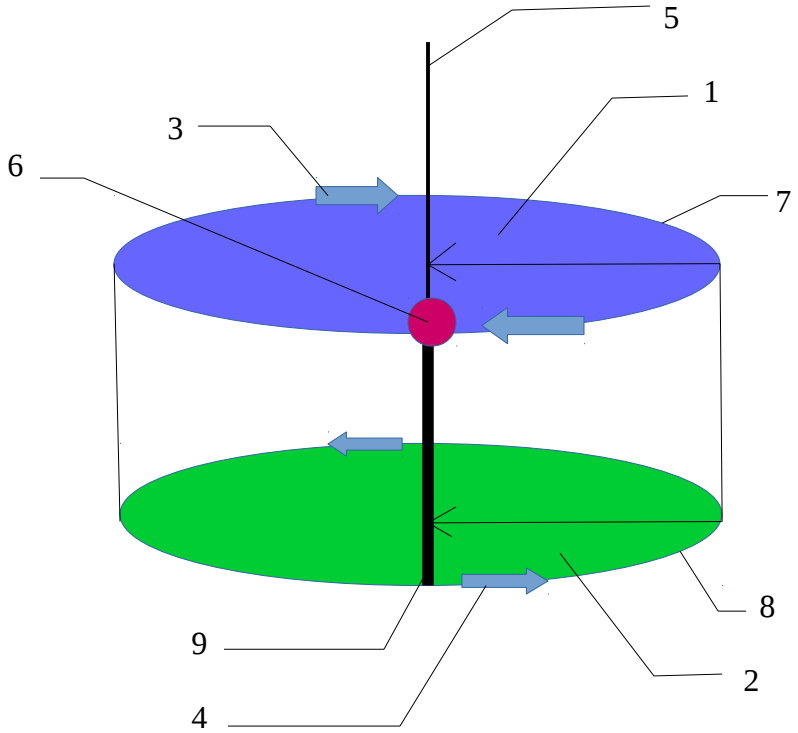


5 packets of 4096 bytes burst with frame sequences of 5.

New Cryptographic Energy Model Design

Chapter 3

Cryptographic Energy Model Visual Design



1. Curvature Motion light Energy
2 Curvature Motion heavy energy
3. Clockwise motion
4. Counter Clockwise Energy Regeneration
5. 1st Data String 256 bits
6. Gateway Check node point
7. Blue Elliptic curve 701 Bits
8. Green Elliptic Curve 709 Bits
9. 2nd Data String 512 Bits

Cryptographic Energy Model Design Method and Process

I will now present a New Cryptographic Energy Design based on Dynamic Heat and Asymmetrical Energy principles and applications. I will be discussing the method and process of this model

As you can see the energy in chart 1-B curvature is represented by shades of blue and green. The 1st curvature uses 701 bits and the 2nd uses 709 for a total of 1410 bits. Depending on the number of cycles used example 9 I can generate 701 * 9 = 6309 bits + 709 * 9 = 6381 bits total 12690 bits. 12609< 20480 The system architecture can only support 20480 bits so the cycles could support 9 cycles.

The Data Strings has the 1st linear string at 512 Bits and the 2nd uses 768. The total is 1280 bits

If I set up a series of arrays we could find the total number of bits based on the following example above

1st Curvature = a1
2nd Curvature = b1
1st data string = c1
2nd data string =d1
a= 6309
rem 1st curvature 701 *9 cycles
b= 6381
rem 2nd curvature 709 * 9 cycles
c = 512
d = 768

array-1 = {a1,b1}
array-2 = {c1,d1}
array-3 = array-1 + array-2
array-3 =12690+1280 = 13970 bits

This system design could support this Cryptographic model because 13970 < 20480 bits

This model uses a combination of both Linear and Curvature motion and Energy equating to a Cryptographic model design as discussed in previous copyrighted models this is being employed and in fact is being improved upon. I would like to add that because I have 6510 bits I could also create a cryptographic password that insures IP Packet Integrity and authenticity example:

1). I can use a Data string of 512 bits create parallel strings name it p1+ and p2- The user chooses either p1+ or p2- and than access the curvature space using a prime number of 701 bits with 7 cycles= 4907 bits. The next step is to add the 512 bits =5409 bits to use for password security. The Equation can be written as follows:

Z {p1+,P2-} = 512 bits Linear

Y = 4907 bits= Curvature

W = Z + Y = 5409

B = W/1
B= W/3
B = W/9

I have created 3 spaces that can be used to break 5409 bits into chunks of data this creates a mechanism for multiple paths the final product is below:

B = 5409/1 = 5409
B = 5409/3 = 1803
B = 5409/9 = 601

To reverse this you simply take the final product * the number being divided example:

5409 /9 = 601
601 * 9 = 5409

If you can reverse the process the password encryption is crackable, The idea is not to create an uncrackable password but to show how I can create a process and method that employs linear and curvature motion along with multiple paths as shown so this also shows The Barry equality Field Equation can be used in a principle application outside of Traditional Physics.

I will provide my final thoughts in the next chapter.

Final Thoughts

Chapter 4

This completes The SS-87 Motherboard Design 3rd generation. I have provided a lot of detail for this project and have included additional material that shows and promotes a password encryption equation and model that employs reverse engineering, linear and Curvature Motion, and multiple paths in chapter three.

I have also used 20480 bits for this design as a constant and boundary to demonstrate the many principles and applications of my designs used in the past.

The visual display of the Hardware components provide detail specifications including data strings.

Thank you for taking the time in reviewing this work ! If you would like to view other works please goto my website below:

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www.barrysscientificbasedproducts.info

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