# Barrys SS-75 Ver 1.4  Motherboard Design

**by**

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## Introduction

Thank you for taking the time in reading this Technological Work. I will be upgrading and adding new features in the Super Sonic 75 Model Design Series. This will be the last upgrade for this series of motherboards.

This work will use a lot of Visual Designs along with a new file and hashing scheme to promote 12288 block data schemes used for IP frames and packet exchanges . I have combined the SS 65 and 75 model Designs to make improvements on this new design itself.

I have updated the previous SS-75 Motherboard Design to include the following:

1). Hardware components added Voltage Regulator, 4/5 Pin Bios, 3072 built in Certificate Rom Chip upgraded video for 192 bit processing of four wires instead of 128 bits in previous designs.

2). Hashing and Algorithm scheme for second layer OSI Data link layer processing with 12288 Character block data with 4 rows by 3072 Characters matrix with 16 frames.

3). 12288 Character Data block tied into the {768 bit address scheme}.

4). 16 layer frame with address entanglement and security

5). 3072 bit built in Hardware Certificate via ROM Chip to insure hardware updates using validation and authentication using TCP connections for updates.

6). One memory stick uses 2 banks with total 4 data strings each with 192 bits total 768 bits for addressing also memory now has an external reserved area of space that now has the capacity to hold 3072 bits instead of 1024 in previous designs.

7). Updated new Cryptographic Model linear and Curvature based Energy with array processing and specs introduced for model design and array processing.

8). Created a Mathematical equation used for Physics, Computer Sciences, and Mathematics named it the **Barrys Dynamic Infinity Loop equation**.

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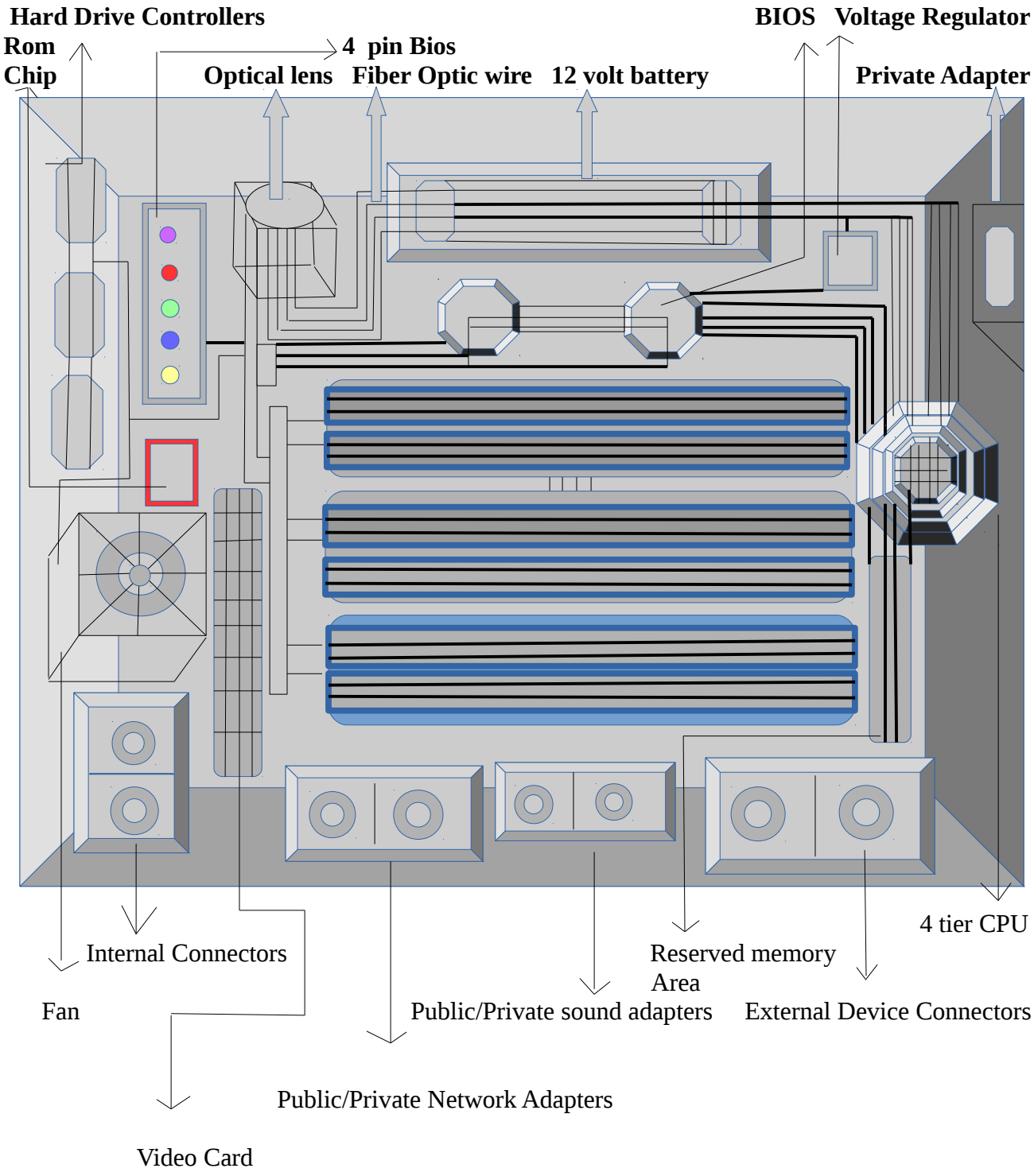
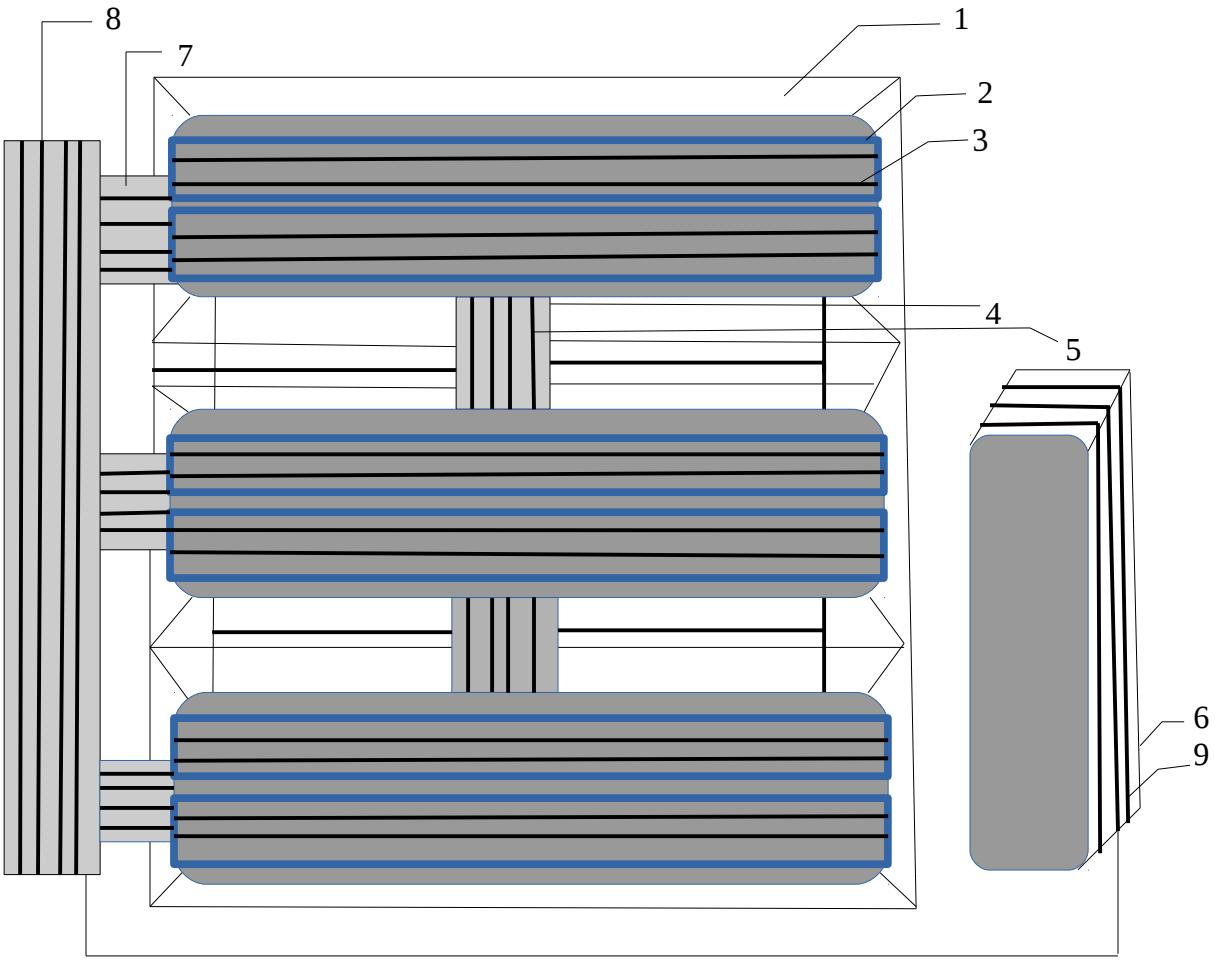
# Chapter 1

# Visual Design

**Model Super Sonic 75 Motherboard- Design Rev 1.4 1-A**

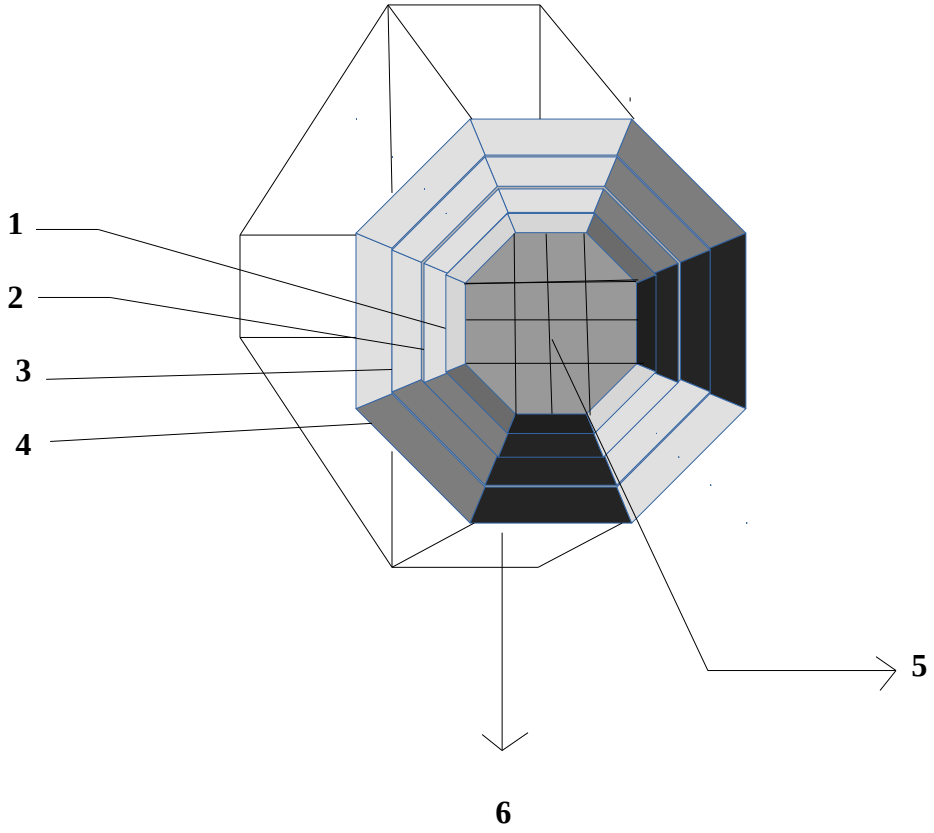


**Model Super Sonic 75 Motherboard- Design Rev 1.4  2-A**



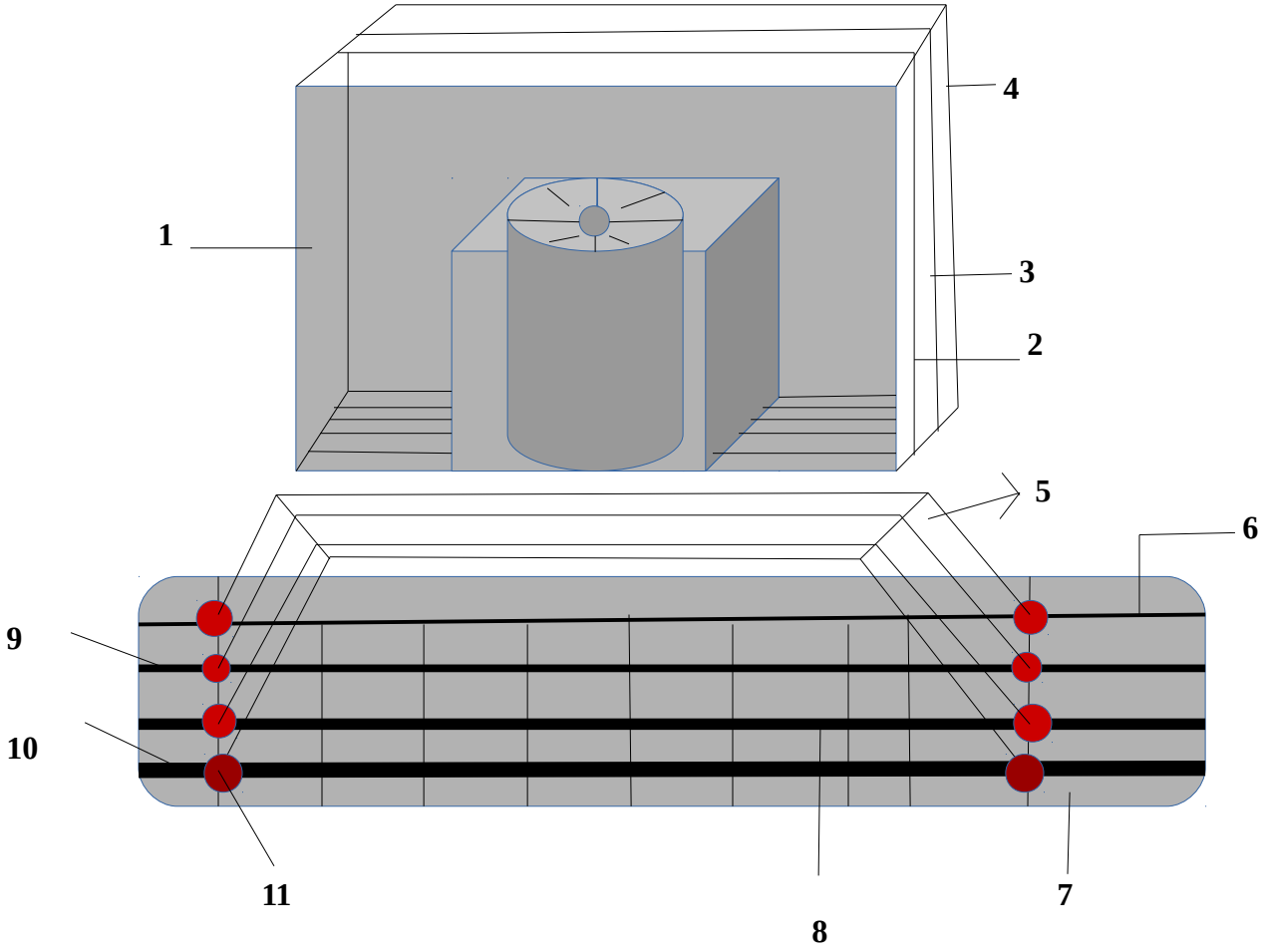

1). Fitting to hold Memory Chips
2). Banks 2 banks per memory chip 384 per bank total 768 bit addressing scheme
3). Data Strings 2 strings per Bank 192 bits per string total 4 strings per chip 768 bit addressing
4). Area Memory Bridge (Bytes to Frames switches)
5). 4 data strings per bridge 192 bits per wire total 768 bits
6). Reserved Memory area (Buffer) 3072 bits
7). Fiber Optic tube address encasement
8). Address Bridge 4 wires 192 bits per wire to process Fiber Optic
9). Three Data wires for holding in reserved space 1024 per wire total 3072 bits.

**Model Super Sonic 75 Motherboard- Design  Rev 1.4 3-A General View**



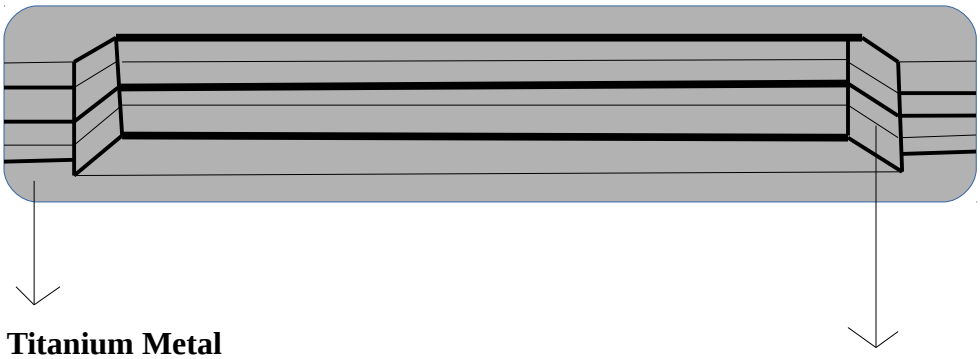

**1). Public CPU Area of Space 4096 Bits**
**2). Private CPU Area of Space 4096 Bits**
**3). Shared CPU Area of Space 4096**
**4). Reserved CPU Area of Space 3072 Bits**
**5). Fiber Optic Net**
**6). CPU Fitting**

**Model Super Sonic 75 Motherboard- Design Rev 1.4 4-A General View**




1). Public Video Area Space
2). Private Video Area Space
3). Shared Video Area Space
4). Reserved Video Area Space
5). Video Data Bride 4 slots
6). Public Data String
7). Titanium video fitting
8). Shared Data String
9). Private Data String
10). Reserved Data String
11). Node Points (End to End point connection)

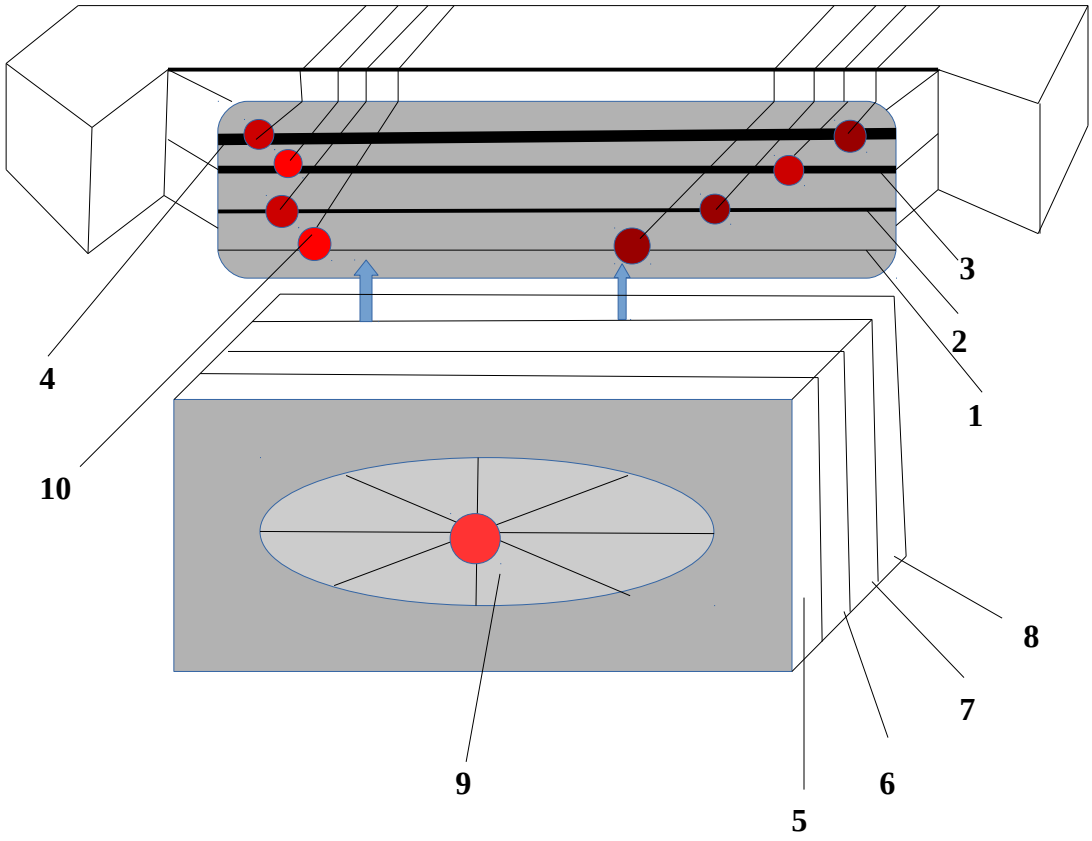
**Model Super Sonic 75 Motherboard- Design  Rev 1.3 5-A General View**



**Titanium Metal**

**Video Card Slot**

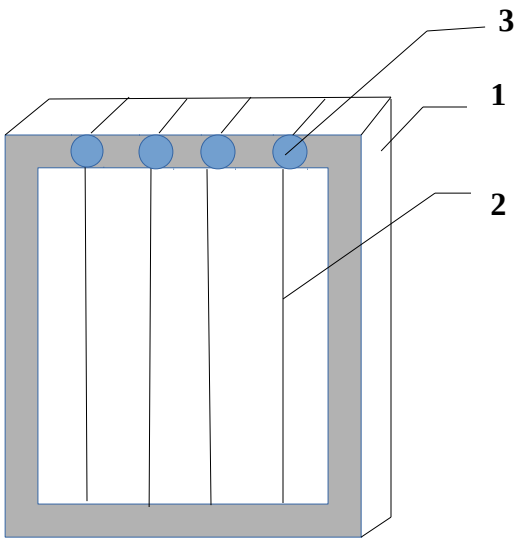
**Model Super Sonic 75 Motherboard- Design  Rev 1.4 6-A General View**




| | |
|---|---|
| 1 | Public Data String 192 bits |
| 2 | Private Data String192 bits |
| 3 | Shared Data String 192 bits |
| 4 | Reserved Data String 192 Bits |
| 5 | Public Video Slot |
| 6 | Private Video Slot |
| 7 | Shared Video Slot |
| 8 | Reserved Video Slot |
| 9 | Video Fan |
| 10 | Node Points |

**Model Super Sonic 75 Motherboard- Design  Rev 1.4 7-A General View**

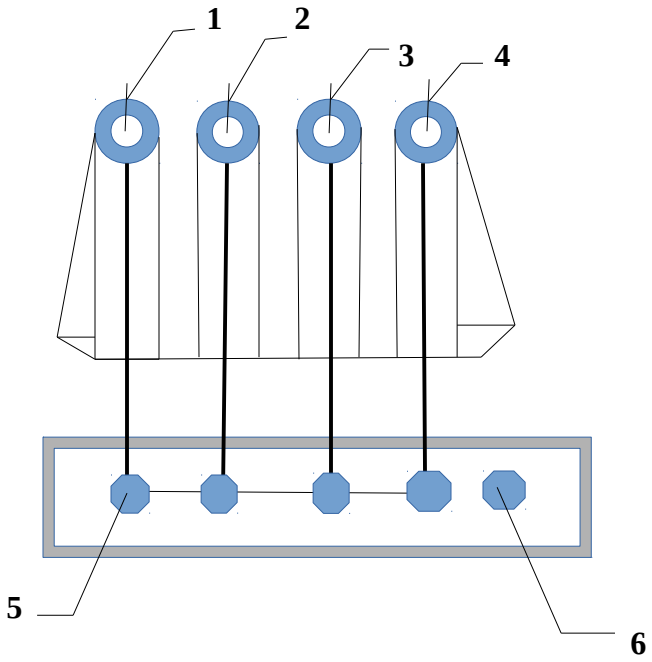
**Voltage Regulator 4 wire Check**




**1). Overall view of chip**
**2). 4 wires inside chip to check flow of voltage 768 bits per wire total 3072 bits**
**3). Node Point check testing wires for on and off conditions**

**Model Super Sonic 75 Motherboard- Design  Rev 1.4 8-A General View**

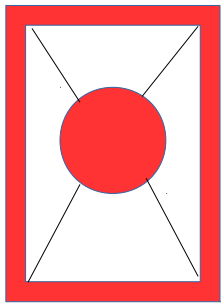
**4/5 Pins Bios**




**1). Public Bios Pin**
**2). Private Bios Pin**
**3). Shared Bios Pin**
**4). Reserved Bios Pin**
**5). Bios Bins that connect to node Points**
**6). Bios Pin Clearing areas of spaces**

**Model Super Sonic 75 Motherboard- Design  Rev 1.4 9-A General View**

**3072 Built in Certificate ROM Chip**



## Overview of Design

I will be going over each new and updated component of the SS 75 Motherboard Design Version 1.4. Chart 1-A provides an overall view of the Model Design. The improvements I made took previous designs of the Models SS 65/75 with the following:

### Chart 1-A

1). Major Components added Voltage Regulator, 4/5 Pin Bios, 3072 built-in Certificate using ROM read only memory chip also upgraded is the reserved area buffer chip for memory using three wires 1024 a piece bringing the total to 3072 bits instead of 1024 in previous designs.

2). The voltage Regulator checks for Electrical spikes 768 bits per wire total 3072 bits.

3). The 4/5 Pin bios is primarily used for clearing out the area of spaces usually to “Pin the bios” it is a 4/5 pin used to clear each area of space the empty or 5th pin is used to slot the pins to clear out all areas of space see chart 8-A.

4). A 3072 Hardware Certificate is built-in via ROM Chip read only being presented to show validation and authentication of Hardware updates are being completed see below through usage of a 3072 bit ROM chip.

**Model Super Sonic 75 Motherboard- Design  Rev 1.4 9-A General View**

Barrys Scientific Based Products 3072 Bit Hardware Verification Certificate

This Certificate is used to check for authenticated Hardware updates it is built into the motherboard via ROM Chip and uses TCP Connections guaranteed packet exchanges.

**Chart 2-A**

Chart 2-A is the component Memory and the improvements I made are the following:

1). Memory sticks now have 2 banks with 4 data strings that are 192 bits a piece for a total of 768 bits this allows for 768 bit addressing. In the past, the most for previous designs was 256 bits. I have updated the reserved area of memory with 3 wires that support 3072 bits instead of 1024

2). As stated previously Memory now has an extra component and space defined as Reserved and uses three wires that allow a total of 3072 bits this allows for more efficient uses of temporary storage used as buffers to prevent overflows and bottlenecks.

3). Memory addresses are now defined as 768 bits and are encased in fiber optics to prevent questionable activities.

**Chart 3-A**

Chart 3-A is the video defined areas of space Public, Private, Shared and reserved. The video card has node points at each end point validating mac addresses within the area of space similar to end to end point communications. Previous designs permitted data strings to constantly check the data string within the device which may create a bottleneck. The video slot also employs a data bride for byte to frame processing for each slot. The Data strings are defined as 192 bits for each space bringing the total to 768 bits.

## Chart 7-A

Chart 7-A is a voltage regulator used to monitor voltage this has 4 wires with 768 bits bringing the total to 3072 bits it also comes with node points used to check on and off status of switches.

## Chart 8-A

Chart 8-A is a hardware component used to pin the bios and clear out areas of spaces it has a total of 5 pins the 4 pins are monitored to check status of node points or switches on or off status. The 5$^{th}$ pin is used to clear the areas since it is not connected to the data string and the other 4 pins.

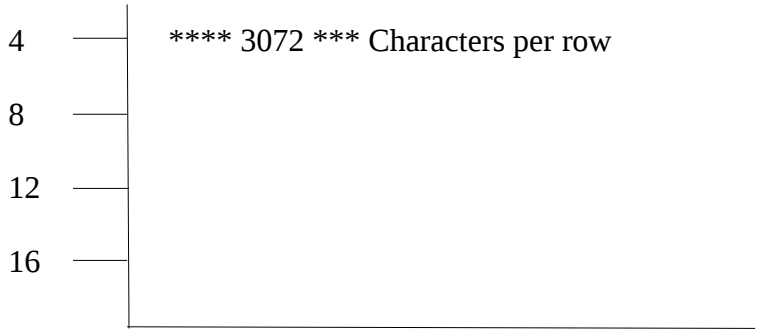
## Chart 9-A

Chart 9-A is a software certificate that is built in the system used for checking authentication and validation of hardware updates when required this uses a TCP connection guaranteed packet updates of hardware components and it is built into the motherboard via ROM Chip to insure data integrity.

# Chapter 2

# Single 12228 Data Block processing

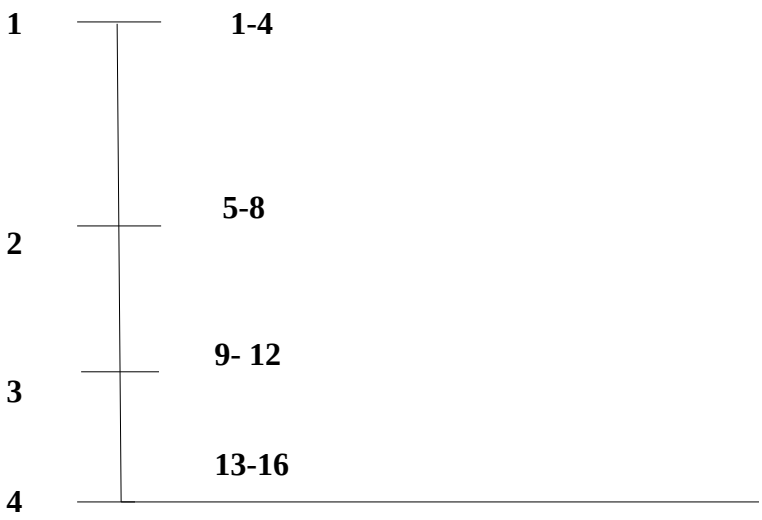
I will begin by defining the block data of 12228 characters with the 768 bit addressing scheme from here I will create a matrix of 4 rows each with 3072 characters matrix. See chart below.




3072 * 4 = 12288

Since I have defined my address scheme as 768 bits. I divide 12288 by 768 bits and it comes up with 16 frames. I divide 16 frames by 4 3072 byte frames in bursts equals 12288 bits. To secure the data when sending outbound to the Internet or Intranet, I use a frame entanglement swapping frame 1 and 2. This is reassembled at the final destination or hop for old timers also this enforces endpoint to endpoint communication. I create four packets of 3072 byte frames equal to 12288 I can take this further by demanding each packet is authenticated with a 3072 bit certificate held in memory to insure data integrity. If you wish to create an even more secure environment, The user chooses which packet order sequencing is to be used see chart below. I could even swap the last frame's of 15 and 16 with final packet assembly reaching the end point of communication.

Packet # Frame sequence




**4 packets of 3072bytes burst with frame sequences of 4.**

# Chapter 3

# Group  Frame to Packet Processing

Please remember the following OSI layer Stack Protocol Frame and Packet Processing

| | |
|---|---|
| Physical | Bits to Bytes |
| **Data Link layer** | **Bytes to Frames** |
| **a). MAC address Layer/Data Link Layer** | **Bytes to Frames** |
| IP layer | Frames to Packets |

The conversion and process is the following:

12288 * 768 Bits = 94347184 bits / 3072 = 3072

The next step is to convert the bits into bytes this is dependent on how you represent characters in fields for example in the 80's you could use 2 bytes or 16 bits to represent 1 character in my presentation this equals 768 bits and I created a 12288 data block or 4 rows of 3072 Character blocks of Data.

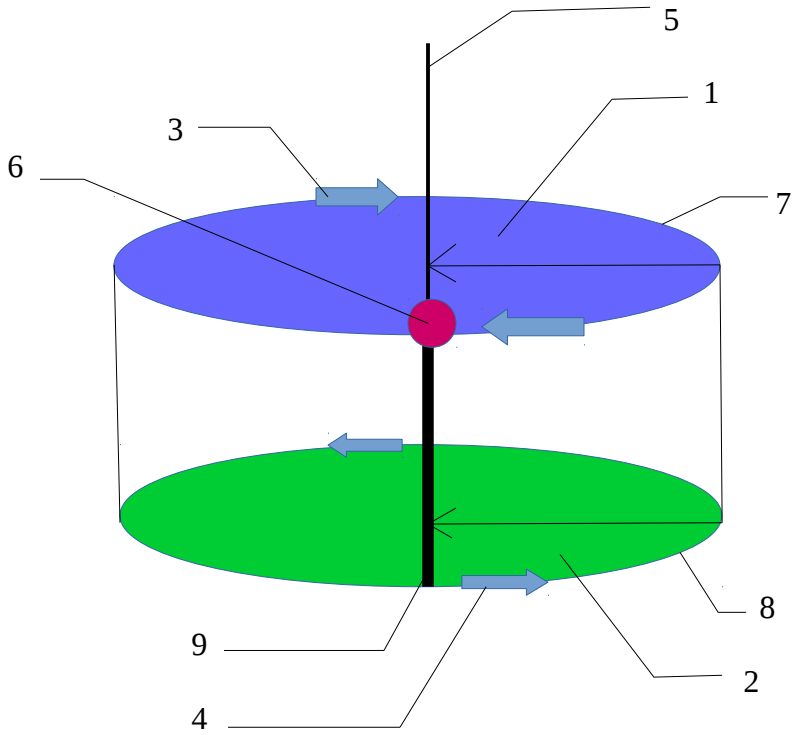
9437184 bits divided by 3072 = 3072 characters / 4 frames 3072 a piece used for sequencing. This equals 3072 and than I select 4 because 3072 * 4 = 12288. The frames can be broken up because on the lower level second layer you create a sub-level within the second layer defining the mac address and how it is going to be used for frames into packets. This is a basic review. If you do not understand this, You may wish to study the OSI 7 layer stack and TCP/IP protocols.

I will now present my new cryptographic model in the next chapter.

# Chapter 4

# New Cryptographic Energy Model Design

**Cryptographic Energy Model Visual Chart 1-B**




1. Curvature Motion light Energy
2 Curvature Motion heavy energy
3. Clockwise motion
4. Counter Clockwise Energy Regeneration
5. 1st Data String 256 bits
6. Gateway Check node point
7. Blue Elliptic curve 701 Bits
8. Green Elliptic Curve 709 Bits
9. 2nd Data String 512 Bits

**Cryptographic Energy Model Design**

I will now present a New Cryptographic Energy Design based on Dynamic Heat/Spectrum along with Asymmetrical Energy principles and applications

As you can see the energy in chart 1-B curvature is represented by shades of blue and green. The 1st curvature uses 701 bits and the 2nd uses 709 for a total of 1410 bits. Depending on the number of cycles {round trips used} example 8 I can generate 701 * 8 = 5608 bits + 709 * 8 = 5672 bits total 11208 bits. 11208 < 16384 curvature space. The system architecture can only support 16384 bits so the cycles could support 8 cycles. I could use 9 cycles 9* 701 = 6309 bits + 709 * 9 =6381 bits total 6309 + 6381 = 12690 bits curvature space + 256 + 512 = 13970. This system could support 9 cycles because 13970 bits < 16384 bits. In these examples I have shown in principal and application that a multi-motion space application is pretty much rendered the theory of 8 times ∏ r2 8 times the infinite loop to be not valid because the variable 8 was used as a constant and placed limitations on infinity. The purpose of this example was to show theory and practical application. I am not placing limitations using defined terms but merely showing why placing constant variables on infinity loops are incorrect and should be replaced with Dynamic based variables that change within the system structure.

The Data Strings has the 1st linear string at 256 Bits and the 2nd uses 512. The total is 768 bits

If I set up a series of arrays we could find the total number of bits based on the following example above

1st Curvature = a
2nd Curvature = b
1st data string = c
2nd data string =d
a= 5608
rem 1st curvature 701 *8 cycles
b= 5672
rem 2nd curvature 709 * 8 cycles
c = 256
d = 512

array-1 = {a,b}
array-1 = {a + b}
array-2 = {c,d}
array-2 = {c + d}
array-3 = {array-1 + array-2}
rem adding linear and curvature arrays
array-3 =11280+768 = 12048 bits

This system design could support this Cryptographic model because it is < 16384 bits

This model uses a combination of both Linear and Curvature motion and Energy equating to a Cryptographic model design and will be employed in **next Generation patent Industrial Designs**.

# Chapter 5

## Barrys  Dynamic Infinity Loop equation

I have completed research on some of the ideas I presented and noticed some individuals used cryptographic constants I deployed on my models examples 15360 and 5120. One such example is a recently deceased Physicist who uses 8 pie G / C $4^{th.}$ **I always believe one good deed deserves another** so I will help those that decided to take my ideas and apply them to their own works without full knowledge of what they are doing. They have broken two rules I have employed the past 10 plus years. They are the following:

1). Energy is Asymmetrical
2). Energy is Dynamic

The problem with the above Equation is that applying constants means you are placing limitations and confinement within the Universe in human terms without full knowledge or observation. In the bible old testament it is written that God told his prophets 1 day = 1000 years to me meaning time is dynamic not constant. In Genesis, it talks of the Earth voided no time or space God formed time and space in this Universe and placed limitations on this Universe laws of nature God also was above time and space so this implies time and space are Dynamic not constant. I have spent 35 plus years in the Martial Arts to understand the difference between Internal and External Energy seen and not seen not constant either. I also understand that to become truly free means freeing your mind not being confined to one system example Korean Martial Arts spent 1981 – 1999 formal training and went on to study different styles and created my own style that works for me hint not limited to one system. The issues with people who place constants do not have full knowledge or observation of things they cannot touch. The equation is below that changes part of the Infinity loop from a constant to a dynamic equation.

$$\text{infinity loop } \infty = \frac{\triangle \prod(g2 - g1)}{\triangle c}$$

**Variables assigned**

 Dynamic metric based number

Π pie

G2 = Internal subatomic paricles

G1 = Newtons Constant

c = speed of light

The number 8 placed limitations on a self defined system and confined space you have no facts or evidence-hard also see my own cryptographic model asymmetry. I changed the constant 8 with a red triangle based on Dynamics of a system one universe may or may not be the same as others so this is shown to be dynamic. G represents Newton's constant so placing gravitation on sub atomic particles that pass through matter is incorrect or not represented properly research indicates no gravitation on subatomic particles. G2 represents Internal Energy and G1 shows External Energy thus measurements of sub atomic and Atomic particles have better representation when dealing with Newton's constant. The 1600's had no knowledge of sub-atomic particles it needs to be updated. The speed of light is another subject that is not very well addressed We have a variable C4 speed of light to the $4^{th}$ power and that is incorrect or not represented very well when dealing with sub-atomic particles that go past the speed of light and pass through our Universe using time and spatial expansion. The issue with this is what happens when One Universe is faster or slower than the other expansion and contraction of space time. I use a Red Triangle to represent Dynamic and represents and recognize spatial expansion and contraction Dynamically. This equation can be used in advanced Physics, Mathematical, and or Computer Science models hint cryptographic. I believe in Intelligent Design God.

The next equation was derived from the equation 8 pie G / C $4^{th}$

The Equation is listed S = ∏ AKC3/ 2hg

The issues with this equation is applying constants on areas of events and dimensional space. This equation did not solve the issue with sub-atomic particles that pass through matter and exceed the speed of light also it has been found that the Newton constant gravitation has no effect on subatomic particles so to apply a constant on universes or black holes that have asymmetrical events is not very reasonable lacks logic. I feel the correct Equation that can be better represented is below

$$S = \frac{\triangle \prod * a\ 2^{nd} * \triangle c}{\triangle ((h2 - h1) * (g2 - g1))}$$

Variables assigned

$\triangle$ = Dynamic metric snapshot

$\prod$ = Pie

A $2^{nd}$ = Multiple event horizons

C = speed of light

h = Planck constant

g2 = Internal Subatomic Particles

g1 = Newtons Constant

As stated before one good deed deserves another so Your models and equations have been shown to be no good and demonstrates not valid. Evidence is pointed against these old listed equations.

# Chapter 6

# Final Thoughts

**Final Thoughts**

I have updated and have developed the SS 75 with the latest version 1.4 Motherboard Design known as Super Sonic. The updates include Voltage Regulator monitor and check voltage, 4/5 Pin Bios used to clear out areas of spaces, 3072 built-in certificate via Rom Chip and 12288 Single and Group Character processing. I have updated the video card slot and it can now process 192 bit data strings total 768 bits. These Strings use Fiber Optic Nets and Titanium.

I have updated memory with the following specs 1 memory stick = two banks with each bank using two data strings for total or 768 bits for the addressing and has a reserved area of 3072 bits with 3 wires built into the chip.

The Cryptographic Model has been updated including array processing and specs number of cycles per elliptic curvature certificates. I previously discussed the idea of memory array processing but decided it would be better that I use in this instance a new cryptographic model design that uses both linear and curvature motion for this instance. The cryptographic model uses asymmetry and dynamic variables to show theory and application.

The node points uses uneven symmetry as far as size and spacing are concerned and limited to avoid system bottlenecks. The Data strings 192 bits use end node points that will be used for data integrity and checking internally.

This will be the last of the SS-75 Motherboard Designs as this has been fully developed. I have completed some test on Certificate development and have created the following implemented in server/client programs

1). PKCS 12 RSA 640/5120  browsers email client programs
2). PGP Certificates 12288 RSA signing 2 sub key encryption placed in browser email client programs.
3). Elliptic Curvature 571 bits browser client programs Ca's and servers.

The reason why this is being brought at is because the ideas I have presented are within reach of achieving after 20 years of using the same protocols, certificates it is time to upgrade.

I have presented a new dynamic infinity loop equation that shows the limitations of classical physics and updates it also,  the cryptographic model I present gives a very good example of Energy being dynamic and asymmetrical.

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03/22/2018

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If you enjoy this work, I would like to invite you to www.barrysscientificbasedproducts.net to read other Scientific works!

Thank you for reading this work.